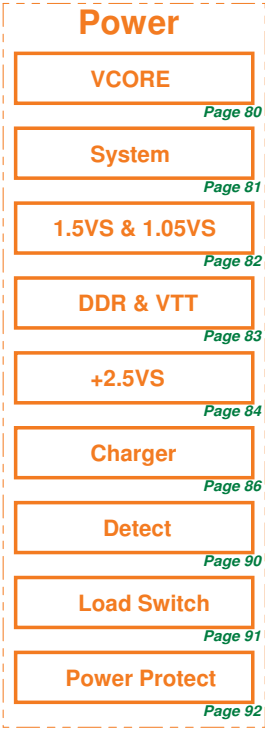
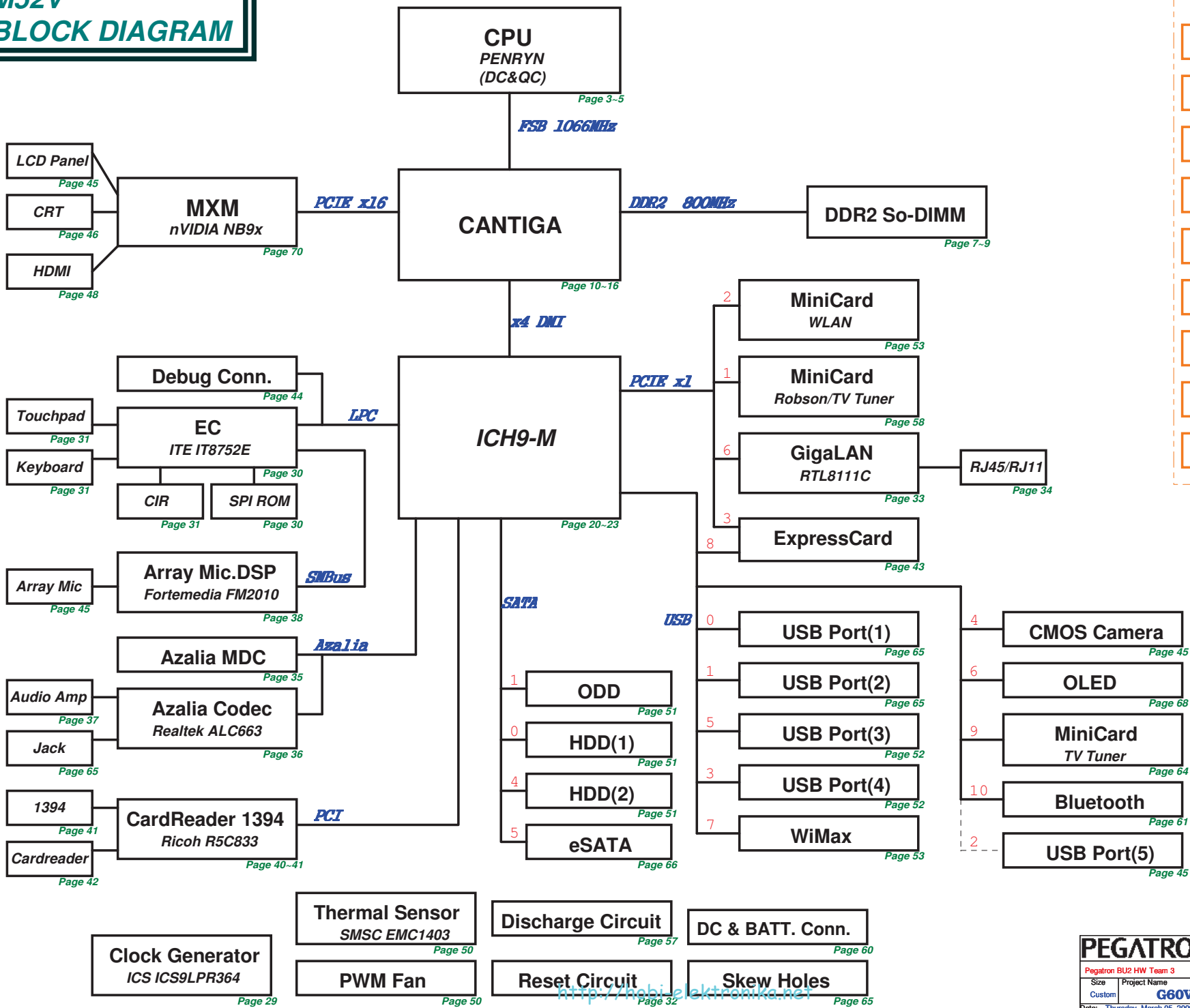


# M52V BLOCK DIAGRAM



## ICH9-M GPIO SETTING

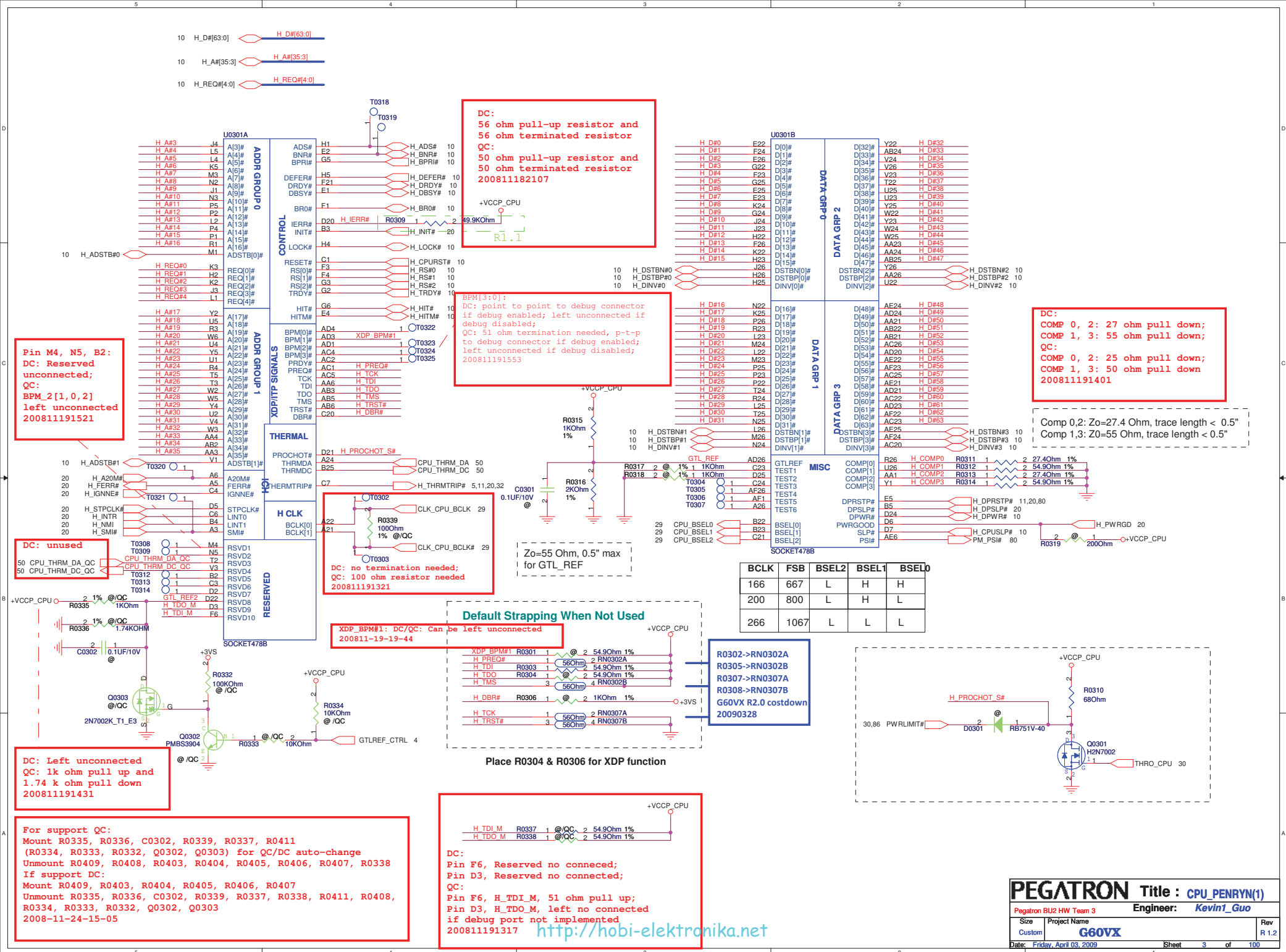
Pin	Pin Name	Signal Name	Type
AG12	BM_BUSY#/GPIO0	PM_BMBUSY#	I
AJ8	TACH1/GPIO1	BT_DECT#	I
F8	PIRQE#/GPIO2	PCI_INTE#	I/OD
G11	PIRQF#/GPIO3	PCI_INTF#	I/OD
F12	PIRQG#/GPIO4	PCI_INTG#	I/OD
B3	PIRQH#/GPIO5	PCI_INTH#	I/OD
AJ9	TACH2/GPIO6		
AH9	TACH3/GPIO7	WLAN_LED_ON	O
AE16	GPIO8	EXT_SMI#	I
AG19	WOL_EN/GPIO9		
AJ24	CLGPIO1/GPIO10		
AG22	SMBALERT#/GPIO11	SMB_ALERT#	I
AC19	GPIO12	EXT_SCI#	I
AH21	GLAN_DOCK#/GPIO13		
AF22	CLGPIO2/GPIO14		
AE20	STP_PC#/GPIO15	STP_PC#	I/O
AJ14	DPRSLPVR/GPIO16	PM_DPRSLPVR	O
AG8	TACH0/GPIO17	WLAN_ON#	O
AH12	GPIO18		
AJ10	GPIO19/SATA1GP		
AE11	GPIO20	BT_LED_ON	O
AJ12	SATA0GP/GPIO21		
AG10	SCLOCK/GPIO22		
E6	LDRQ1#/GPIO23		
AJ27	CLGPIO0/GPIO24		
AG18	STP_CPU#/GPIO25	STP_CPU#	O
AH27	S4_STATE#/GPIO26		
AH25	QRT_STATE0/GPIO27	BT_ON#	O
AD16	QRT_STATE1/GPIO28	CB_SD#	O
AG17	OC#5/GPIO29	INT_USB_OC#	I
AD12	OC#6/GPIO30	INT_USB_OC#	I
AJ18	OC#7/GPIO31	INT_USB_OC#	I
AH11	CLKRUN#/GPIO32	PM_CLKRUN#	O
AE10	AZ_DOCK_EN#/GPIO33		
AG14	AZ_DOCK_RST#/GPIO34		
AG13	SATACLKREQ#/GPIO35		
AF11	SATA2GP/GPIO36	EMAIL_LED#	O
AG11	SATA3GP/GPIO37	PCB_ID0	I
AF9	SLOAD/GPIO38	PCB_ID1	I
AJ11	SDATAOUT0/GPIO39	PCB_ID2	I
AG16	OC#1/GPIO40	USB_CON01_OC#	I
AG15	OC#2/GPIO41	USB_CON23_OC#	I
AE15	OC#3/GPIO42	USB_CON23_OC#	I
AF15	OC#4/GPIO43	NEWCARD_OC#	I
AD10	SATAOUT1/GPIO48		
AG29	CPUPWRGD/GPIO49	H_PWRGD	O
E18	REQ1#/GPIO50	PCI_REQ#1	I/O
C18	GNT1#/GPIO51		
B19	REQ2#/GPIO52	PCI_REQ#2	I/O
F18	GNT2#/GPIO53		
A11	REQ3#/GPIO54	PCI_REQ#3	I/O
C10	GNT3#/GPIO55		

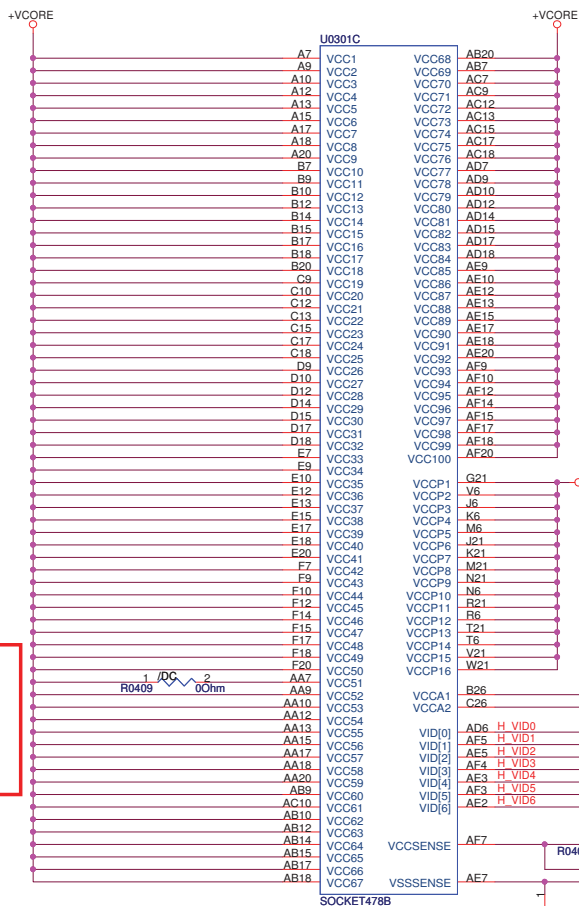
## EC IT8512E GPIO SETTING

Pin	Pin Name	Signal Name	Type	Pin	Pin Name	Signal Name	Type
28	PWM0/GPA0	PWR_LED_UP#	O	105	CLKRUN#/GPH0	PM_CLKRUN#	I/O
29	PWM1/GPA1	CHG_LED_UP#	O	106	CRX1/GPH1	3G_ON#	O
32	PWM2/GPA2			107	CTX1/GPH2	3G_LED_ON#	O
33	PWM3/GPA3			108	GPH3	BAT_LEARN	I/O
34	PWM4/GPA4	LCD_BL_PWM	O	109	GPH4		
35	PWM5/GPA5	FAN_PWM	O	110	GPH5	NUM_LED	O
36	PWM6/GPA6			111	GPH6	CAP_LED	O
38	PWM7/GPA7			74	ADC0/GPI0	NV_OVERT#	I
122	RXD/GPB0	CHG_EN#	O	75	ADC1/GPI1	SUS_PWRGD	I
123	TXD/GPB1	PRECHG	O	76	ADC2/GPI2	ALL_SYS_PWRGD	I
139	CTX0/GPB2			77	ADC3/GPI3	CPU_PWRGD	I
124	SMCLK0/GPB3	SMB0_CLK	I/O	78	ADC4/GPI4	PWR_MON	I
125	SMDAT0/GPB4	SMB0_DAT	I/O	79	ADC5/GPI5	ALS_DA	I
142	GA20/GPB5	A20GATE	O	80	ADC6/GPI6		
4	KBRST#/GPB6	RC_IN#	O	81	ADC7/GPI7		
126	GPB7	PM_RSMRST#	O	84	DAC0/GPJ0	EC_CLK_EN	
133	CRX0/GPC0	CRX0	I	85	DAC1/GPJ1	PM_PWROK	
129	SMCLK1/GPC1	SMB1_CLK	I/O	86	DAC1/GPJ2		
130	SMDAT1/GPC2	SMB1_DAT	I/O	87	DAC1/GPJ3		
64	GPC3	PM_PWRBTN#	O	88	DAC1/GPJ4		
136	WUI2/GPC4	AC_IN_OC#	I	89	DAC1/GPJ5		
65	GPC5	OP_SD#	O	15	GPK0		
140	WUI3/GPC6	BAT1_IN_OC#	I	16	GPK1		
20	GPC7	RFON_SW#	I	17	GPK2		
22	WUI0/GPD0	PWRLIMIT#	I	18	GPK3		
25	WUI1/GPD1	PM_SUSC#	I	48	GPK4		
26	WUI4/GPD2	BUF_PLT_RST#	I	49	GPK5		
27	ECSCI#/GPD3	EXT_SCI#	O	62	GPK6		
19	GPD4	EXT_SMI#	O	63	GPK7		
37	GPD5	LCD_BACKOFF#	O	90	GPL0		
53	TACH0 / GPD6	FAN0_TACH	I	91	GPL1		
54	GPD7			92	GPL2		
23	GPE0	VSUS_ON	O	93	GPL3		
94	GPE1	SUSC_EC#	O	119	GPL4		
95	GPE2	SUSB_EC#	O	120	GPL5		
96	GPE3	CPU_VRON	O	134	GPL6		
141	PWRSW/GPE4	PWR_SW#	I	135	GPL7		
39	WUI5/GPE5	BAT2_IN_OC#	I				
21	GPE6	LID_SW#	I				
24	GPE7	INSTANT_ON#	I				
97	PS2CLK0/GPF0						
98	PS2DAT0/GPF1	COLOREN#	I				
99	PS2CLK1/GPF2	MARATHON#	I				
100	PS2DAT1/GPF3	DISTP#	I				
101	PS2CLK2/GPF4	TP_CLK	I/O				
102	PS2DAT2/GPF5	TP_DAT	I/O				
131	SMCLK2/GPF6	THRO_CPU	O				
132	SMDAT2/GPF7	TP_LED	O				
118	WUI7/GPG0						
121	GPG1	PM_SUSB#	I				
112	GPG2						
116	GPG6						

<http://hobi-elektronika.net>

<b>PEGATRON</b>		<b>Title : System Setting</b>	
Pegatron BU2 HW Team 3		Engineer: <b>Kevin1_Guo</b>	
Size Custom	Project Name <b>G60VX</b>		Rev R 1.2
Date: Thursday, March 05, 2009		Sheet	2 of 100





Pin AA7:  
DC: Power pin  
to VCCP;  
QC: BR1#, for  
debug, should  
left as NC

Pin AC8/AA8/D8:  
DC: VSS to GND;  
QC: Reserved and should be left unconnected,  
but can be rout open for future use  
2008-11-19-21-00

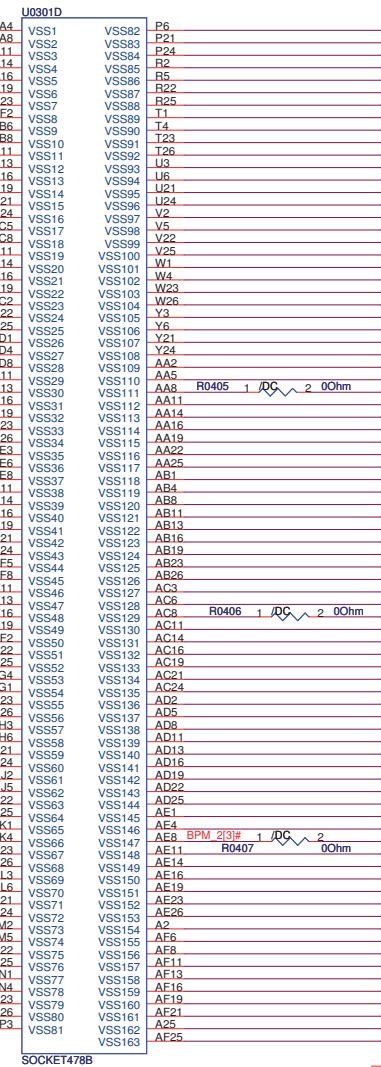
Pin F8:  
DC: VSS;  
QC: GTLREF\_CONTROL, control signal to  
connect or disconnect GTLREF\_2 circuit  
to switch between QC and DC.  
Use this signal to control GTLREF\_2 circuit  
or Use R0335/R0334 voltage divider  
(with the later method, DC and QC will has  
a BOM change)  
2008-11-19-20-55

3 GTLREF\_CTRL ← 1 @QC 2 GTLREF\_CTRL\_R  
R0406 00hm

unmount C0401  
change RNX0401 RNX0402 to short land  
G60VX R2.0 costdown 20090328

Pin AE8:  
DC: VSS to GND;  
QC: BPM\_2[3]#, left  
unconnected

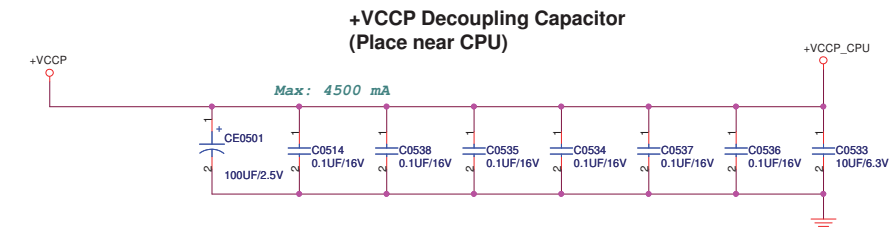
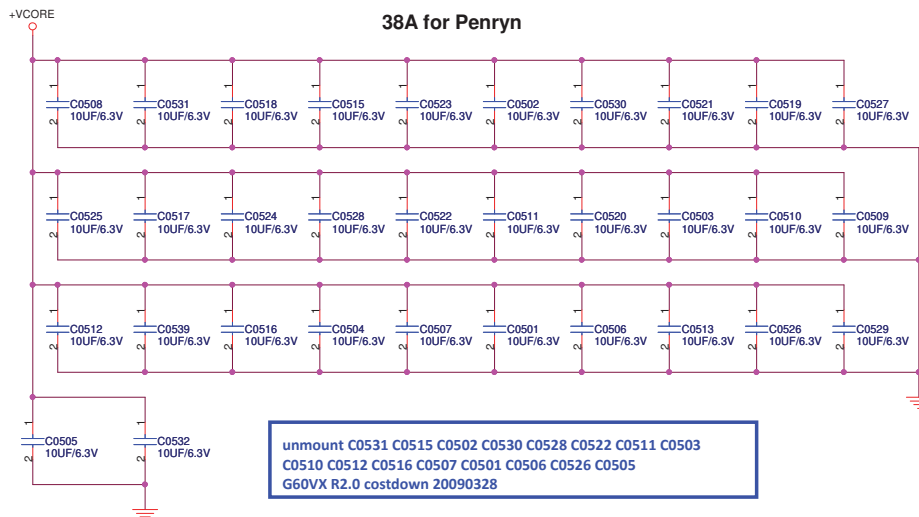
VCCSENSE and VSSSENSE are wide trace  
can't use a RES A to costdown



Reserved, unmounted  
+VCCP\_CPU  
510hm  
R0411  
BPM\_2[3]#

If support DC:  
Mount R0409, R0403, R0404, R0405, R0406, R0407  
Unmount R0335, R0336, C0302, R0339, R0337, R0338, R0411, R0408  
For support QC:  
Mount R0335, R0336, C0302, R0339, R0337, R0338, R0411  
Unmount R0409, R0408, R0403, R0404, R0405, R0406, R0407 ??  
200811122108

??  
<http://hobi-elektronika.net>



**Decoupling guide from Intel**

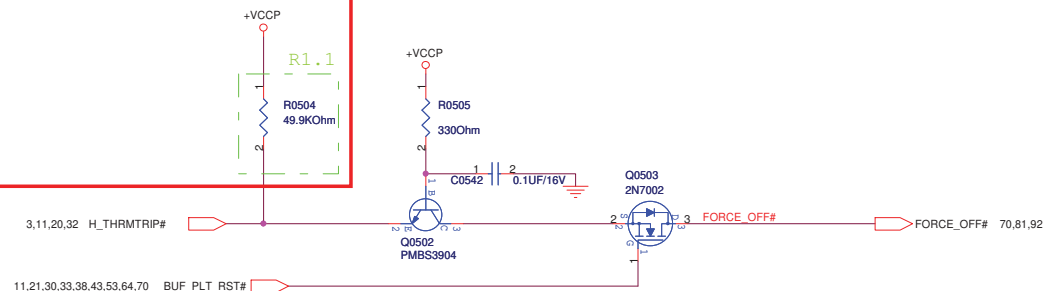
VCORE	22uF/10V r 10uF	* 32pcs
	330uF/2V	* 6pcs
VCCP	0.1uF	* 6pcs
	150uF	* 1pcs ?
	10uF	* 1pcs ?

unmount or delete C0538 C0537 C0536  
G60VX R2.0 costdown 20090328

**+VCORE Mid-Frequency Capacitor**  
Intel: 22uF \*32  
F3S: 10uF \*16  
A7S: 10uF \*10 ....11/17  
V1V: ?

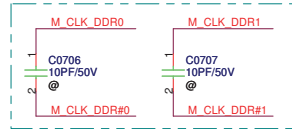
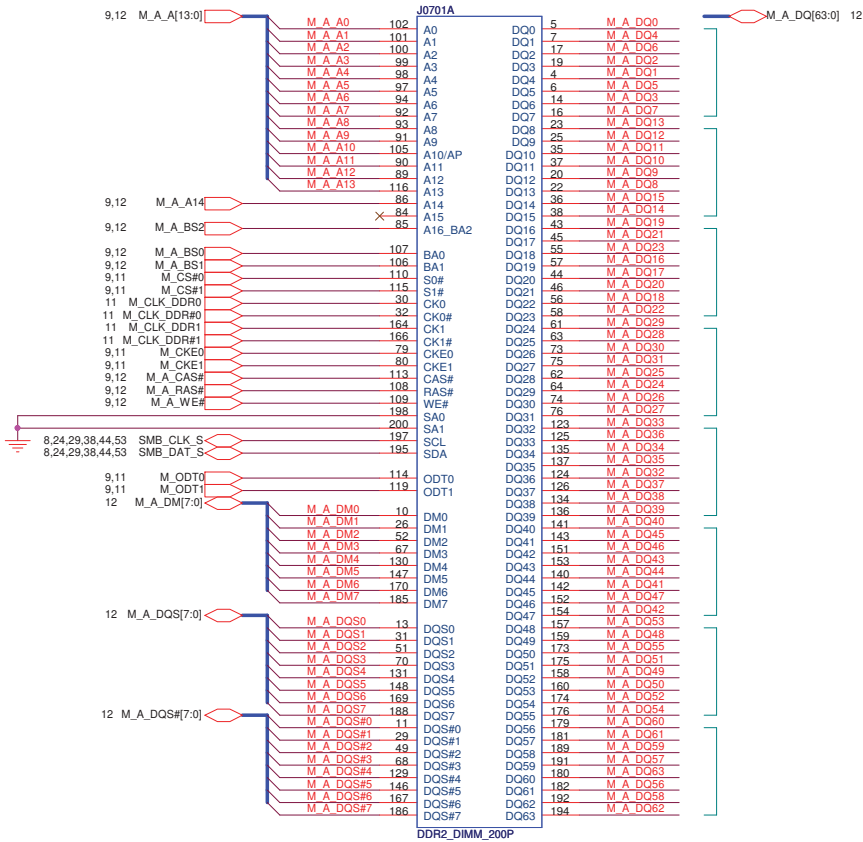
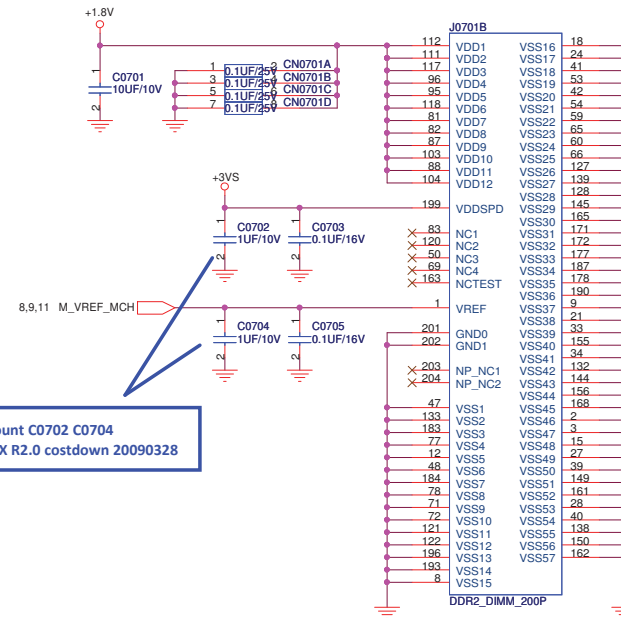
**+VCCP Decoupling Capacitor**  
Intel: 270uF \*1, 0.1uF \*6  
F3S: 100uF \*1, 0.1uF \*4  
V1V: ?

Checklist recommends THERMTRIP# pull up in the CPU side although functionality not used;  
DC: 56 ohm pull up, 55 ohm terminate;  
QC: 50 ohm pull up, 50 ohm terminate  
200811190902

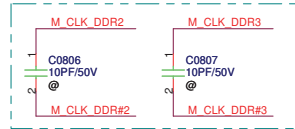
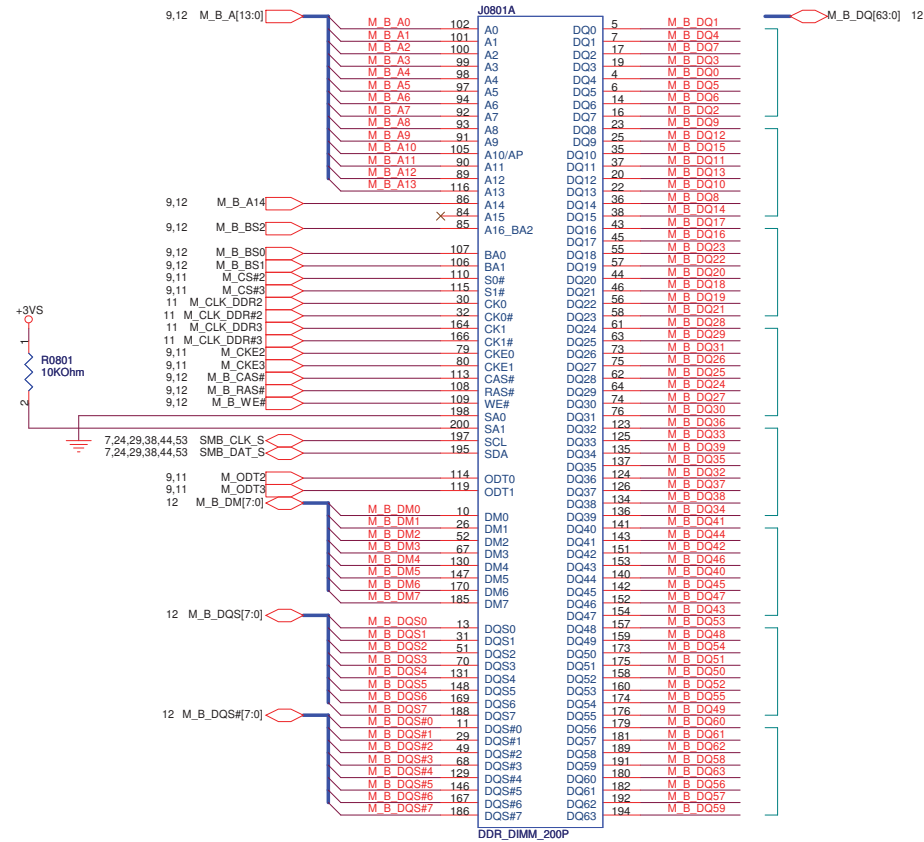
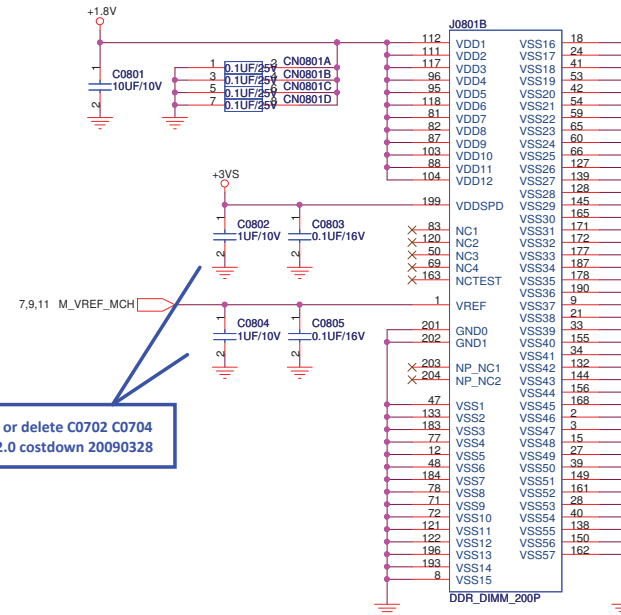


unmount R0504 R0505 C0542 Q0502 Q0503  
connect H\_THRMTRIP# to SB to costdown  
G60VX R2.0 costdown 20090328

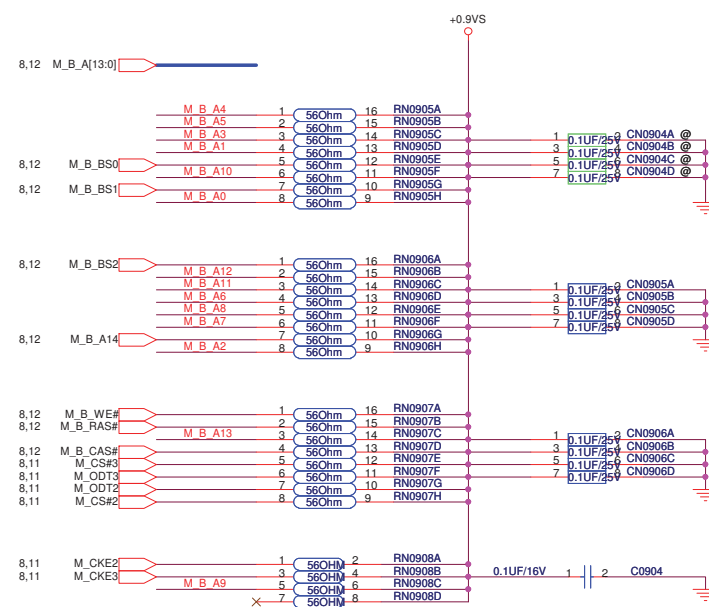
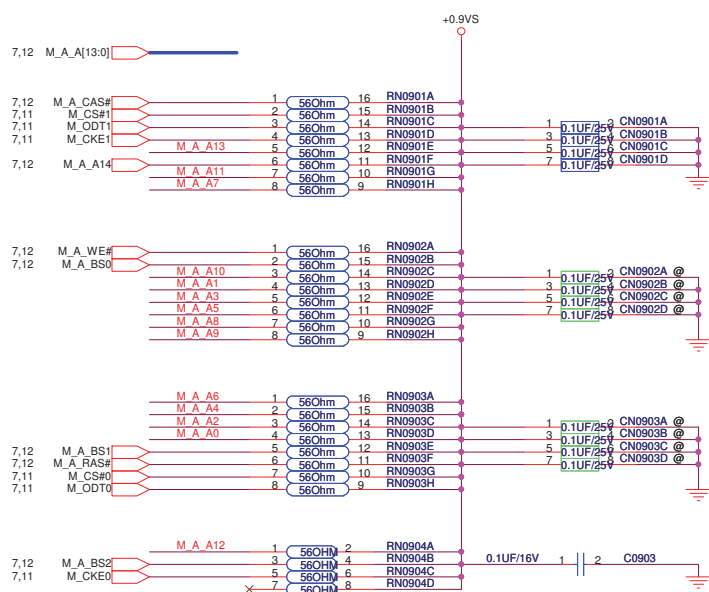
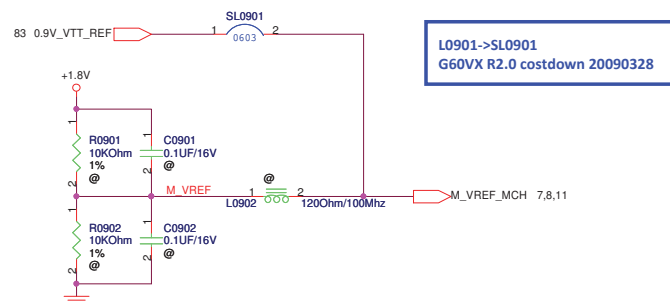
Reserved for 3G

Reverse Type  
H = 9.2 mmunmount C0702 C0704  
G60VX R2.0 costdown 20090328

Reserved for 3G

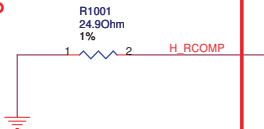
Reverse Type  
H = 4.0 mmunmount or delete C0702 C0704  
G60VX R2.0 costdown 20090328



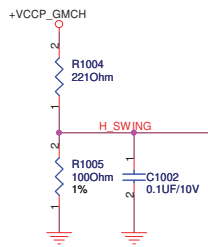




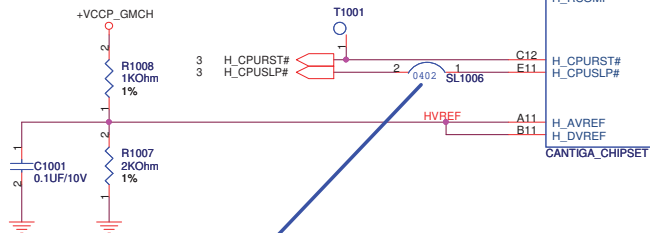
**H\_RCOMP:**  
 DC: 25 ohm pull down;  
 QC: 17 ohm pull down  
 2008-11-19-20-25



**H\_SWING:**  
 DC: 221 ohm pull up,  
 100 ohm pull down;  
 QC: 221 ohm pull up,  
 75 ohm pull down  
 2008-11-19-20-27



Cap 0.1uF within 100 mils from GMCH



RX1006->SL1006;  
 G60VX R2.0 costdown 20090405

U1001A

H_D#0	F2	H_D#_0	A14	H_A#3
H_D#1	G8	H_D#_1	C15	H_A#4
H_D#2	F8	H_D#_2	F16	H_A#5
H_D#3	E6	H_D#_3	H13	H_A#6
H_D#4	G2	H_D#_4	C18	H_A#7
H_D#5	H6	H_D#_5	M16	H_A#8
H_D#6	H2	H_D#_6	J13	H_A#9
H_D#7	F6	H_D#_7	P16	H_A#10
H_D#8	D4	H_D#_8	R16	H_A#11
H_D#9	H3	H_D#_9	N17	H_A#12
H_D#10	M9	H_D#_10	M13	H_A#13
H_D#11	M11	H_D#_11	E17	H_A#14
H_D#12	J1	H_D#_12	P17	H_A#15
H_D#13	J2	H_D#_13	G20	H_A#16
H_D#14	N12	H_D#_14	B19	H_A#17
H_D#15	J6	H_D#_15	E20	H_A#18
H_D#16	P2	H_D#_16	J16	H_A#19
H_D#17	L2	H_D#_17	H16	H_A#20
H_D#18	R2	H_D#_18	J20	H_A#21
H_D#19	N9	H_D#_19	L17	H_A#22
H_D#20	L6	H_D#_20	A17	H_A#23
H_D#21	M5	H_D#_21	B17	H_A#24
H_D#22	J3	H_D#_22	L16	H_A#25
H_D#23	N2	H_D#_23	C21	H_A#26
H_D#24	R1	H_D#_24	J17	H_A#27
H_D#25	N5	H_D#_25	H20	H_A#28
H_D#26	N6	H_D#_26	B18	H_A#29
H_D#27	P13	H_D#_27	K17	H_A#30
H_D#28	N8	H_D#_28	B20	H_A#31
H_D#29	L7	H_D#_29	F21	H_A#32
H_D#30	N10	H_D#_30	K21	H_A#33
H_D#31	M3	H_D#_31	L20	H_A#34
H_D#32	Y3	H_D#_32		
H_D#33	AD14	H_D#_33		
H_D#34	Y6	H_D#_34		
H_D#35	Y10	H_D#_35		
H_D#36	Y12	H_D#_36		
H_D#37	Y14	H_D#_37		
H_D#38	Y7	H_D#_38		
H_D#39	W2	H_D#_39		
H_D#40	AA8	H_D#_40		
H_D#41	Y9	H_D#_41		
H_D#42	AA13	H_D#_42		
H_D#43	AA9	H_D#_43		
H_D#44	AA11	H_D#_44		
H_D#45	AD11	H_D#_45		
H_D#46	AD10	H_D#_46		
H_D#47	AD13	H_D#_47		
H_D#48	AE12	H_D#_48		
H_D#49	AE9	H_D#_49		
H_D#50	AA2	H_D#_50		
H_D#51	AD8	H_D#_51		
H_D#52	AA3	H_D#_52		
H_D#53	AD3	H_D#_53		
H_D#54	AD7	H_D#_54		
H_D#55	AE14	H_D#_55		
H_D#56	AE3	H_D#_56		
H_D#57	AC1	H_D#_57		
H_D#58	AE3	H_D#_58		
H_D#59	AC3	H_D#_59		
H_D#60	AE11	H_D#_60		
H_D#61	AE8	H_D#_61		
H_D#62	AG2	H_D#_62		
H_D#63	AD6	H_D#_63		

HOST

H_A#_3	A14	H_A#3
H_A#_4	C15	H_A#4
H_A#_5	F16	H_A#5
H_A#_6	H13	H_A#6
H_A#_7	C18	H_A#7
H_A#_8	M16	H_A#8
H_A#_9	J13	H_A#9
H_A#_10	P16	H_A#10
H_A#_11	R16	H_A#11
H_A#_12	N17	H_A#12
H_A#_13	M13	H_A#13
H_A#_14	E17	H_A#14
H_A#_15	P17	H_A#15
H_A#_16	G20	H_A#16
H_A#_17	B19	H_A#17
H_A#_18	E20	H_A#18
H_A#_19	J16	H_A#19
H_A#_20	H16	H_A#20
H_A#_21	J20	H_A#21
H_A#_22	L17	H_A#22
H_A#_23	A17	H_A#23
H_A#_24	B17	H_A#24
H_A#_25	L16	H_A#25
H_A#_26	C21	H_A#26
H_A#_27	J17	H_A#27
H_A#_28	H20	H_A#28
H_A#_29	B18	H_A#29
H_A#_30	K17	H_A#30
H_A#_31	B20	H_A#31
H_A#_32	F21	H_A#32
H_A#_33	K21	H_A#33
H_A#_34	L20	H_A#34
H_A#_35		

H_ADS#	H12	H_ADS#	3
H_ADSTB#_0	B16	H_ADSTB#_0	3
H_ADSTB#_1	G17	H_ADSTB#_1	3
H_BNR#	A9	H_BNR#	3
H_BPRI#	E11	H_BPRI#	3
H_BREQ#	G12	H_BREQ#	3
H_DEFER#	E3	H_DEFER#	3
H_DBSY#	B10	H_DBSY#	3
HPLL_CLK	AH7	CLK_MCH_BCLK#	29
HPLL_CLK#	AH6	CLK_MCH_BCLK#	29
H_DPWR#	J11	H_DPWR#	3
H_DRDY#	E9	H_DRDY#	3
H_HIT#	H9	H_HIT#	3
H_HITM#	E12	H_HITM#	3
H_LOCK#	H11	H_LOCK#	3
H_TRDY#	C3	H_TRDY#	3

H_DINV#_0	J8	H_DINV#0	3
H_DINV#_1	L3	H_DINV#1	3
H_DINV#_2	Y13	H_DINV#2	3
H_DINV#_3	Y1	H_DINV#3	3

H_DSTBN#_0	L10	H_DSTBN#0	3
H_DSTBN#_1	M7	H_DSTBN#1	3
H_DSTBN#_2	AA5	H_DSTBN#2	3
H_DSTBN#_3	AE6	H_DSTBN#3	3

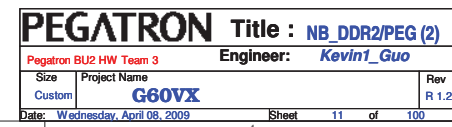
H_DSTBP#_0	L9	H_DSTBP#0	3
H_DSTBP#_1	M8	H_DSTBP#1	3
H_DSTBP#_2	AA6	H_DSTBP#2	3
H_DSTBP#_3	AE5	H_DSTBP#3	3

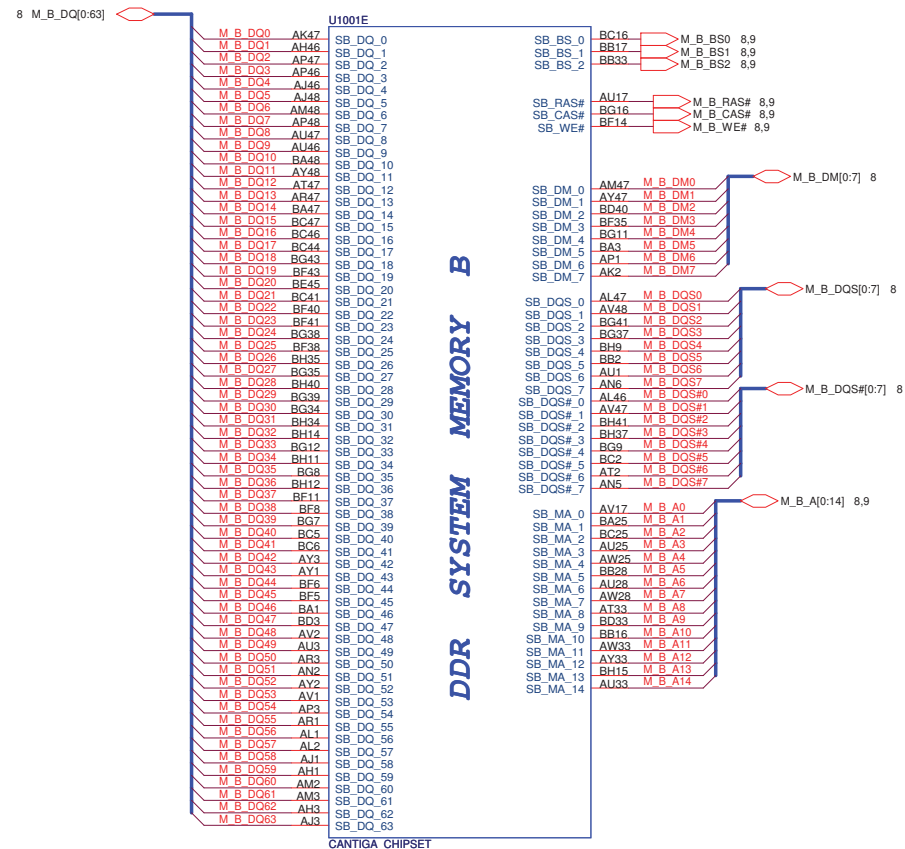
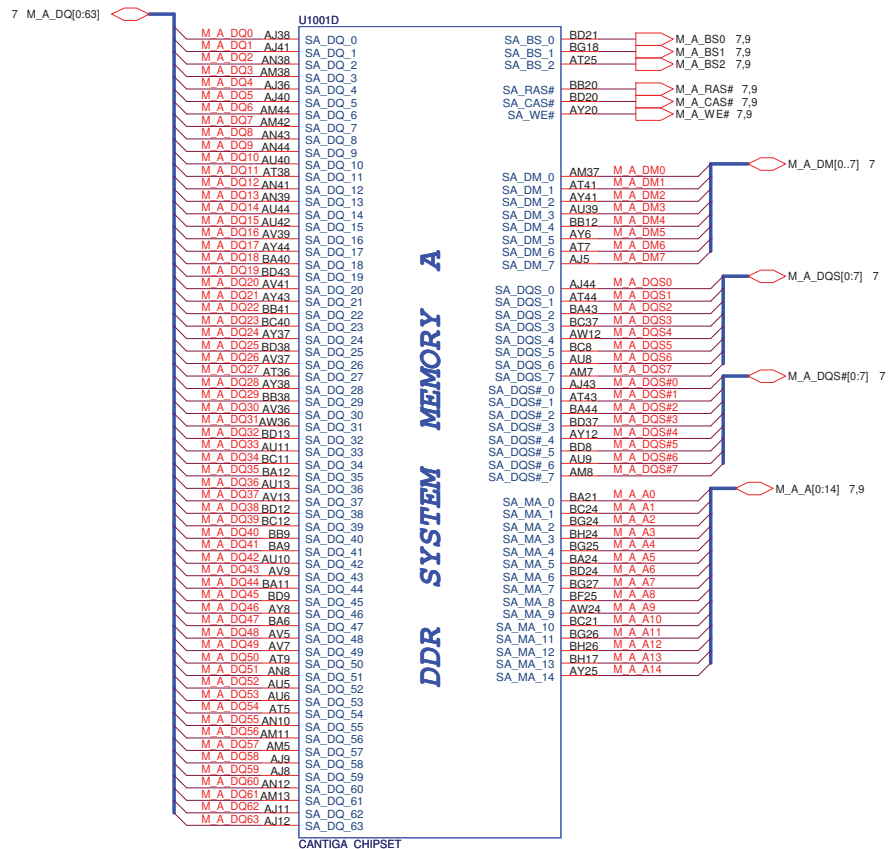
  

H_REQ#_0	B15	H_REQ#0	3
H_REQ#_1	K13	H_REQ#1	3
H_REQ#_2	F13	H_REQ#2	3
H_REQ#_3	B13	H_REQ#3	3
H_REQ#_4	B14	H_REQ#4	3

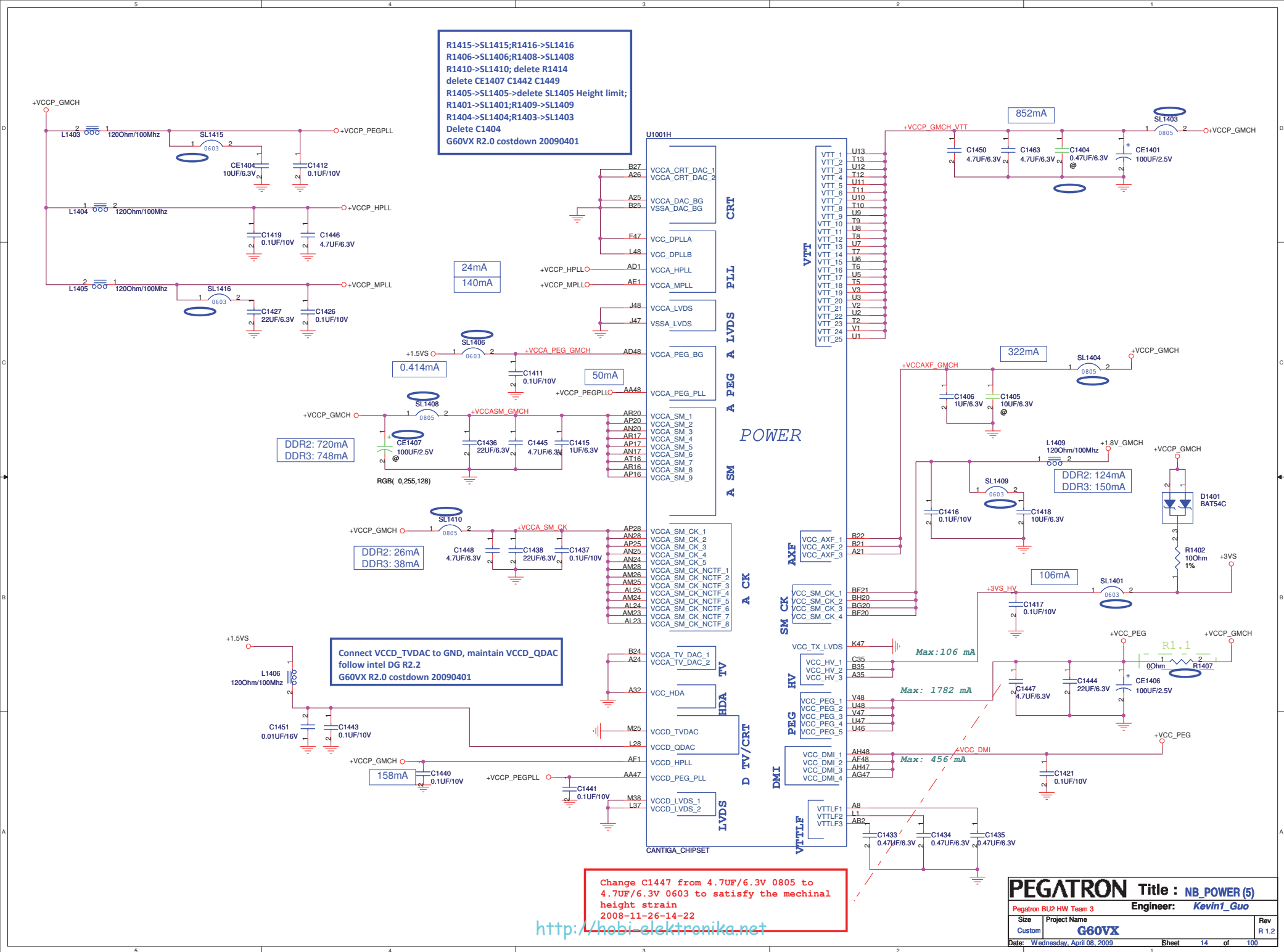
  

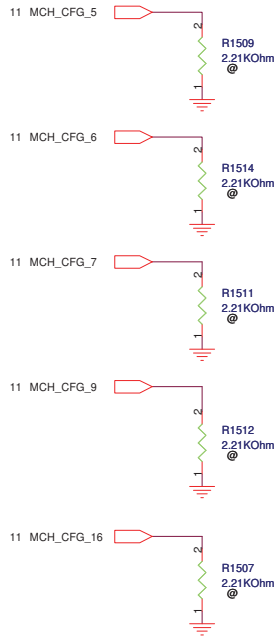
H_RS#_0	B6	H_RS#0	3
H_RS#_1	F12	H_RS#1	3
H_RS#_2	C8	H_RS#2	3











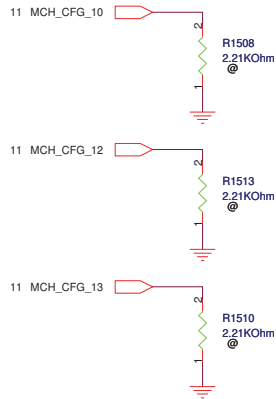
**CFG5 : DMI STRAP**  
**HIGH = DMI X 4 (Default)**  
**LOW = DMI X 2**

**CFG6 : Integrated TPM Host Interface**  
**HIGH = iTPM disable (Default)**  
**LOW = iTPM enable**

**CFG7 : Intel ME Crypto Strap Transport Layer Security cipher suite**  
**HIGH = With confidentiality (Default)**  
**LOW = Without confidentiality**

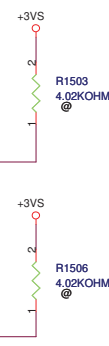
**CFG9 : PCIE GRAPHIC LANE**  
**HIGH = Normal Operation (Default)**  
**LOW = Reverse Lanes**

**CFG16 : FSB Dynamic ODT**  
**HIGH = Enable (Default)**  
**LOW = Disable**



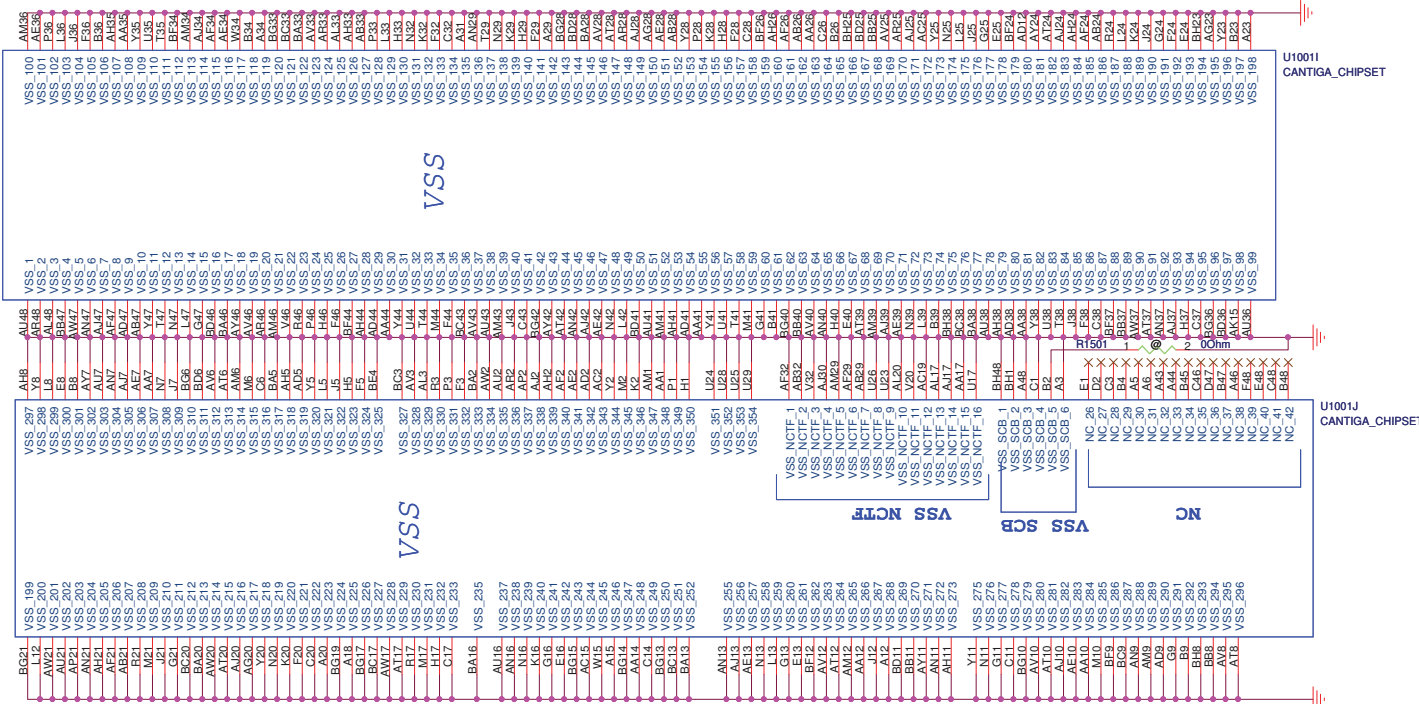
**CFG10 : PCIe Loopback**  
**HIGH = Disable (Default)**  
**LOW = Enable**

**CFG [13:12] : XOR/ALL-Z**  
**00 = Reserved**  
**01= XOR Mode Enabled**  
**10= All-Z Mode Enabled**  
**11= Normal Operation (Default)**

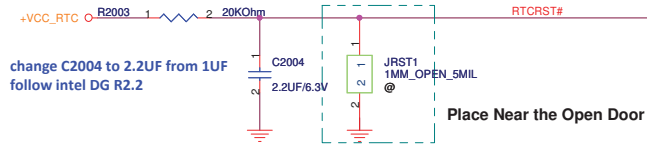


**CFG19 : DMI Lane Reversal**  
**LOW = NORMAL (default)**  
**HIGH = Reverse Lanes**

**CFG20 : SDVO/PCIE CONCURRENT MODE**  
**LOW = ONLY SDVO or PCIE is Operational (Default)**  
**HIGH = SDVO and PCIE are operating simultaneously via the PEG port**

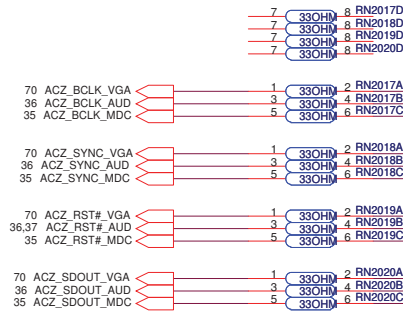




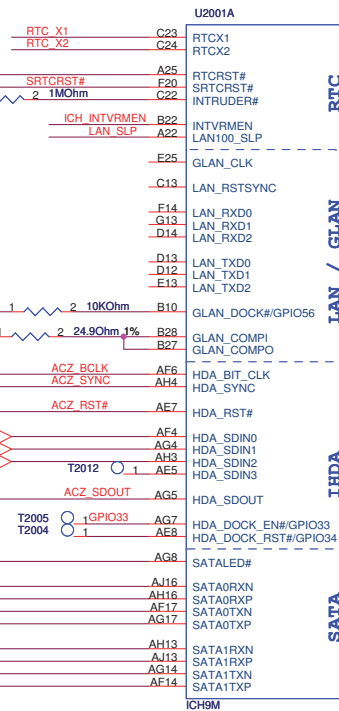
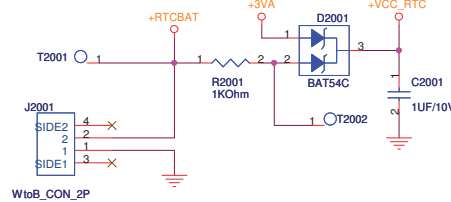
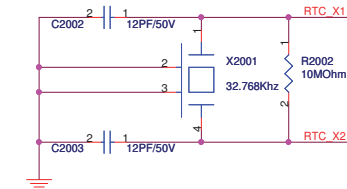
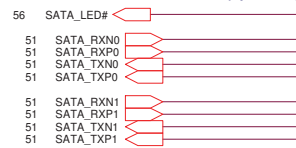


T2010 1 +VCC\_RTC  
T2011 1 RTCRST#

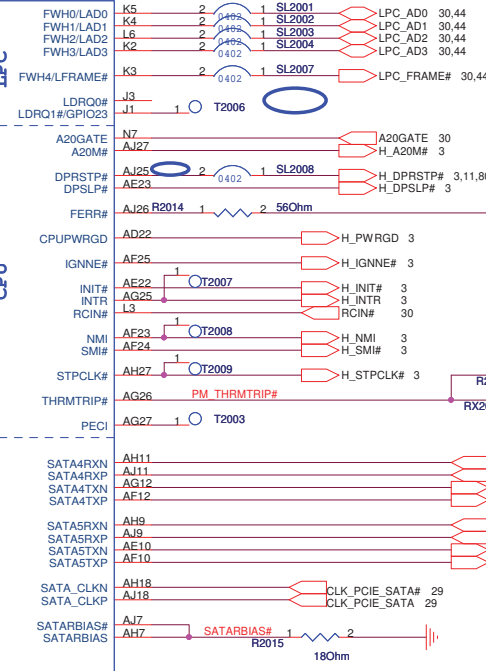
delete R2008 C2005  
RX2017,RX2010,RX2009->RN2017  
RX2018,RX2011,RX2012->RN2018  
RX2019,RX2013,RX2014->RN2019  
RX2020,RX2015,RX2016->RN2020  
G60VX R2.0 costdown 20090401



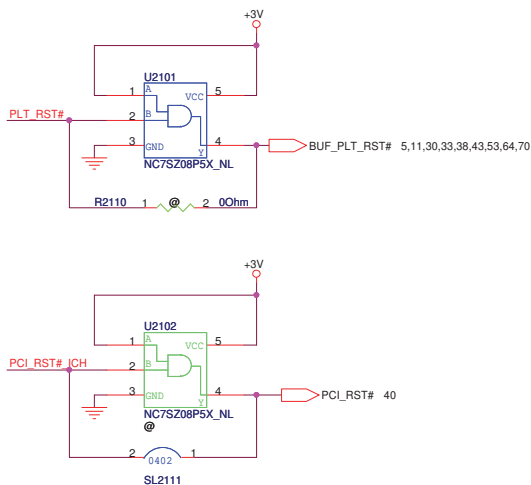
Unmount  
RX2009, RX2012, RX2014, RX2016  
J3501, R3409, R3410, J3401,  
May need change J3402  
For Modem Delete  
20081107



change RX2001,RX2002,RX2003,RX2004  
RX2007,RX2008 to short land  
change reserved RX2005 to SL2005  
G60VX R2.0 costdown 20090401



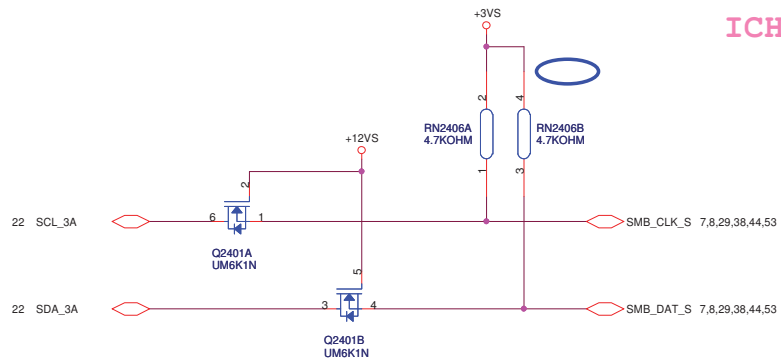




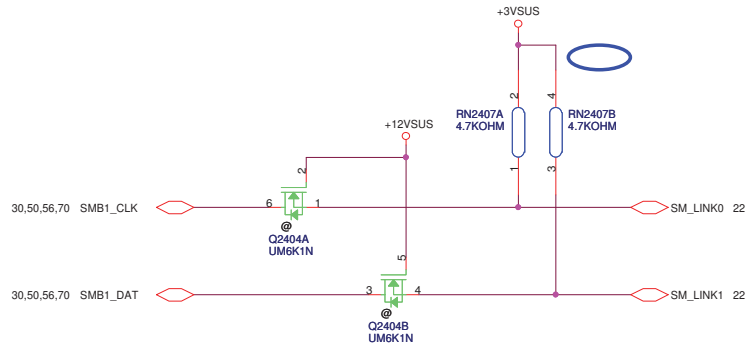
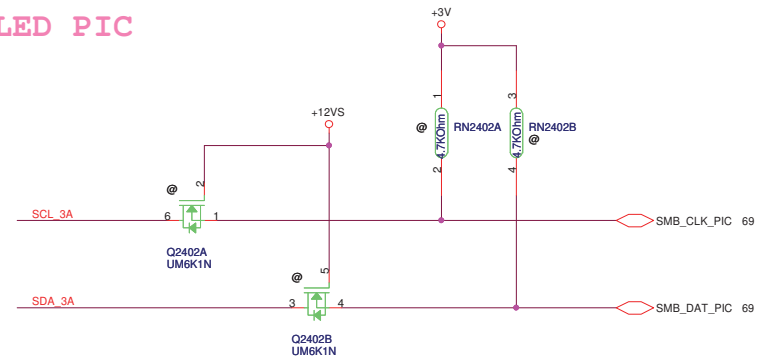
<b>PEGATRON</b>		<b>Title :</b> <i>SB_ICH9M(2)</i>	
<b>Pegatron BU2 HW Team 3</b>		<b>Engineer:</b> <i>Kevin1_Guo</i>	
<b>Size</b> Custom	<b>Project Name</b> <i>G60VX</i>	<b>Rev</b> R 1.2	
<b>Date:</b> <i>Wednesday, April 08, 2009</i>	<b>Sheet</b> <i>21</i>	<b>of</b> <i>100</i>	







## LED PIC



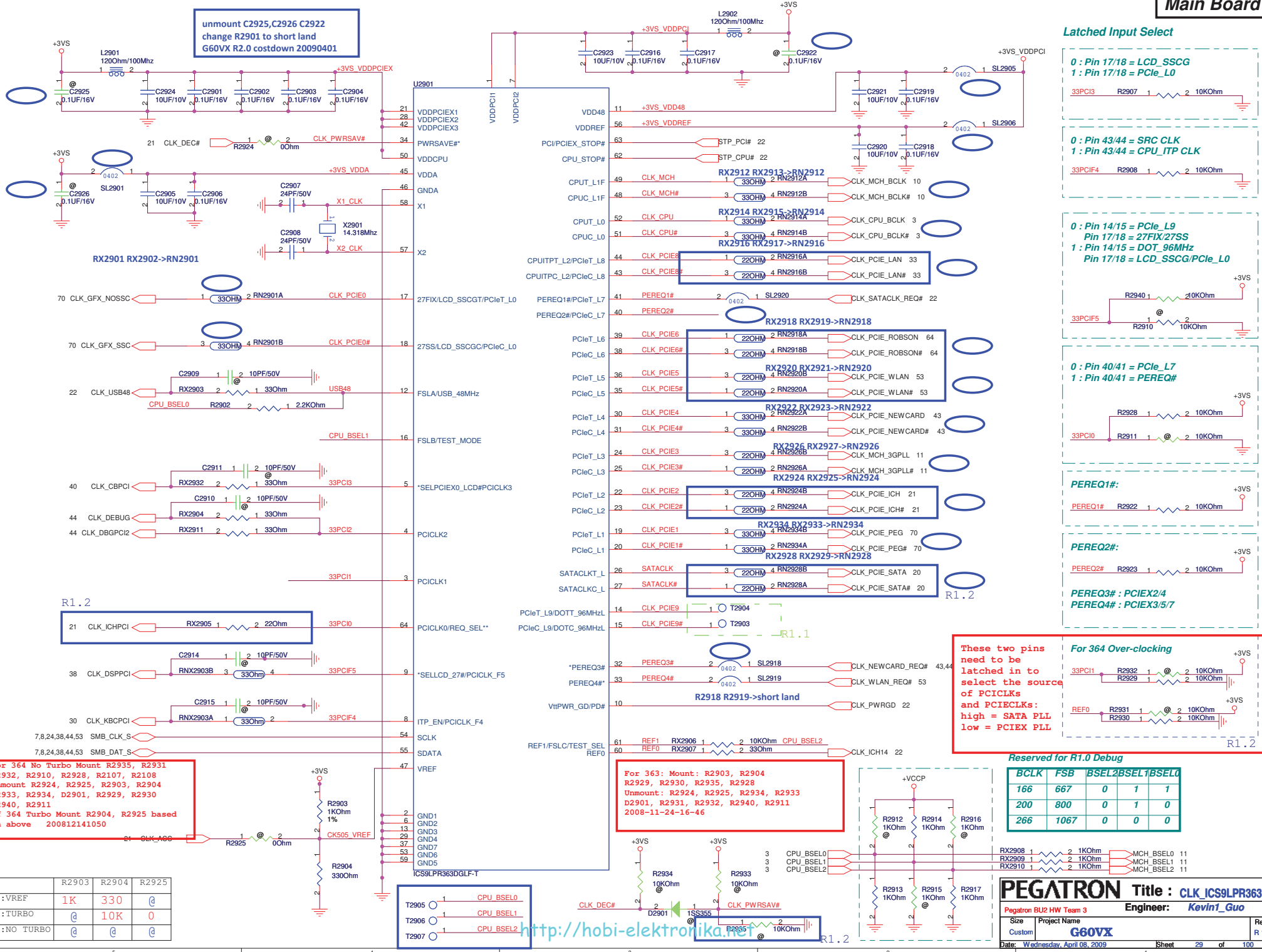
delete R2406 R2405; add RN2406  
delete R2407 R2408; add RN2407  
G60VX R2.0 costdown 20090401

<http://hobi-elektronika.net>

PEGATRON		Title : SB_ICH9M-Other	
Pegatron BU2 HW Team 3		Engineer: Kevin1_Guo	
Size	Project Name	Rev	
Custom	G60VX	R 1.2	
Date: Thursday, April 02, 2009	Sheet	24	of 100

### Latched Input Select

unmount C2925,C2926 C2922  
change R2901 to short land  
G60VX R2.0 costdown 2009040



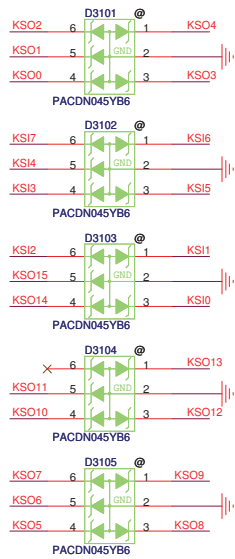
These two pins need to be latched in to select the source of PCICLKs and PCIECLKs:  
high = SATA PLL  
low = PCIEX PLL

**For 364 Over-clocking**

BCLK	FSB	BSEL2	BSEL1	BSEL0
166	667	0	1	1
200	800	0	1	0
266	1067	0	0	0

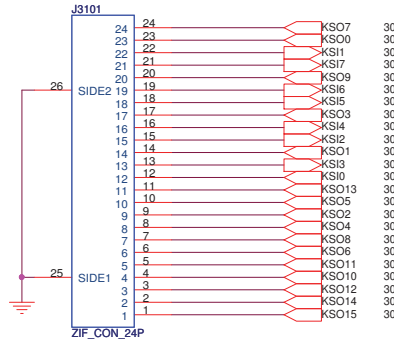
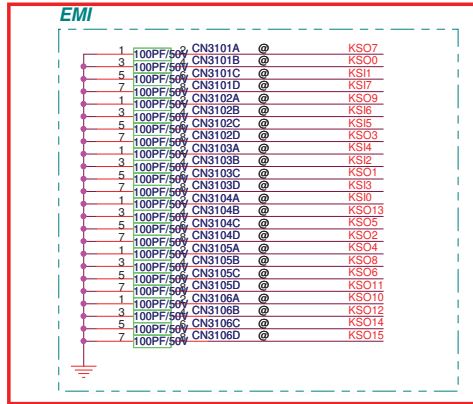






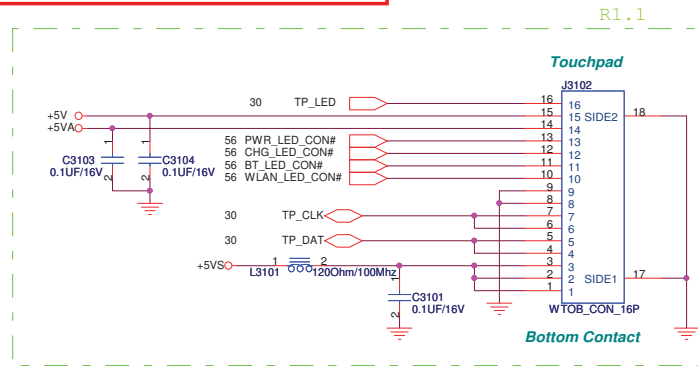
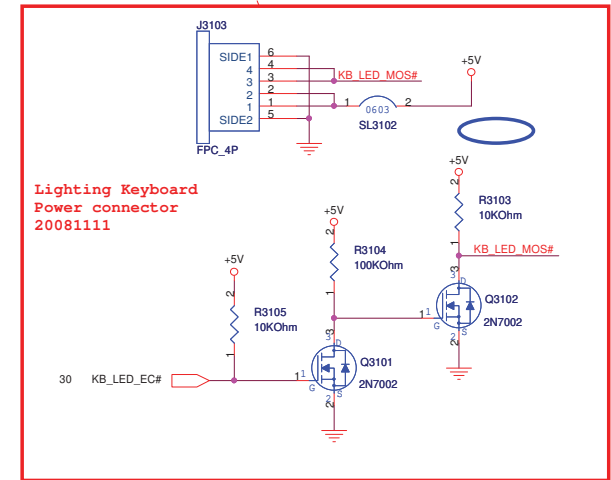
G50VX R1.1 Change back  
20090113

Keyboard

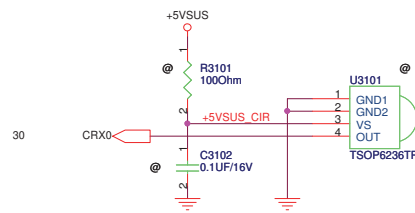


FPC\_4P Reference P/N  
12G183100402

change R3102 to 0603 short land  
G60VX R2.0 costdown 20090401



CIR



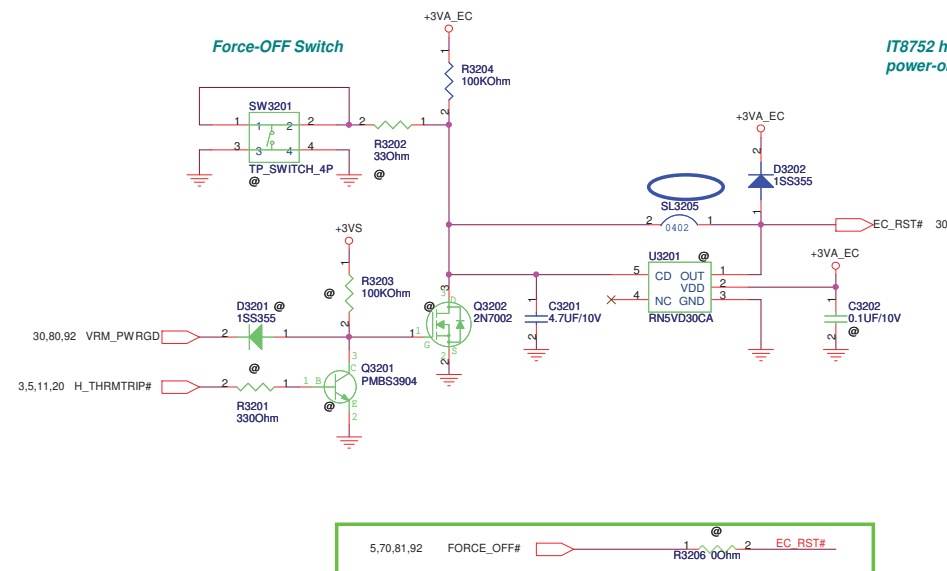
Unmount U3101  
R3101, C3102 For  
delete CIR  
20081107



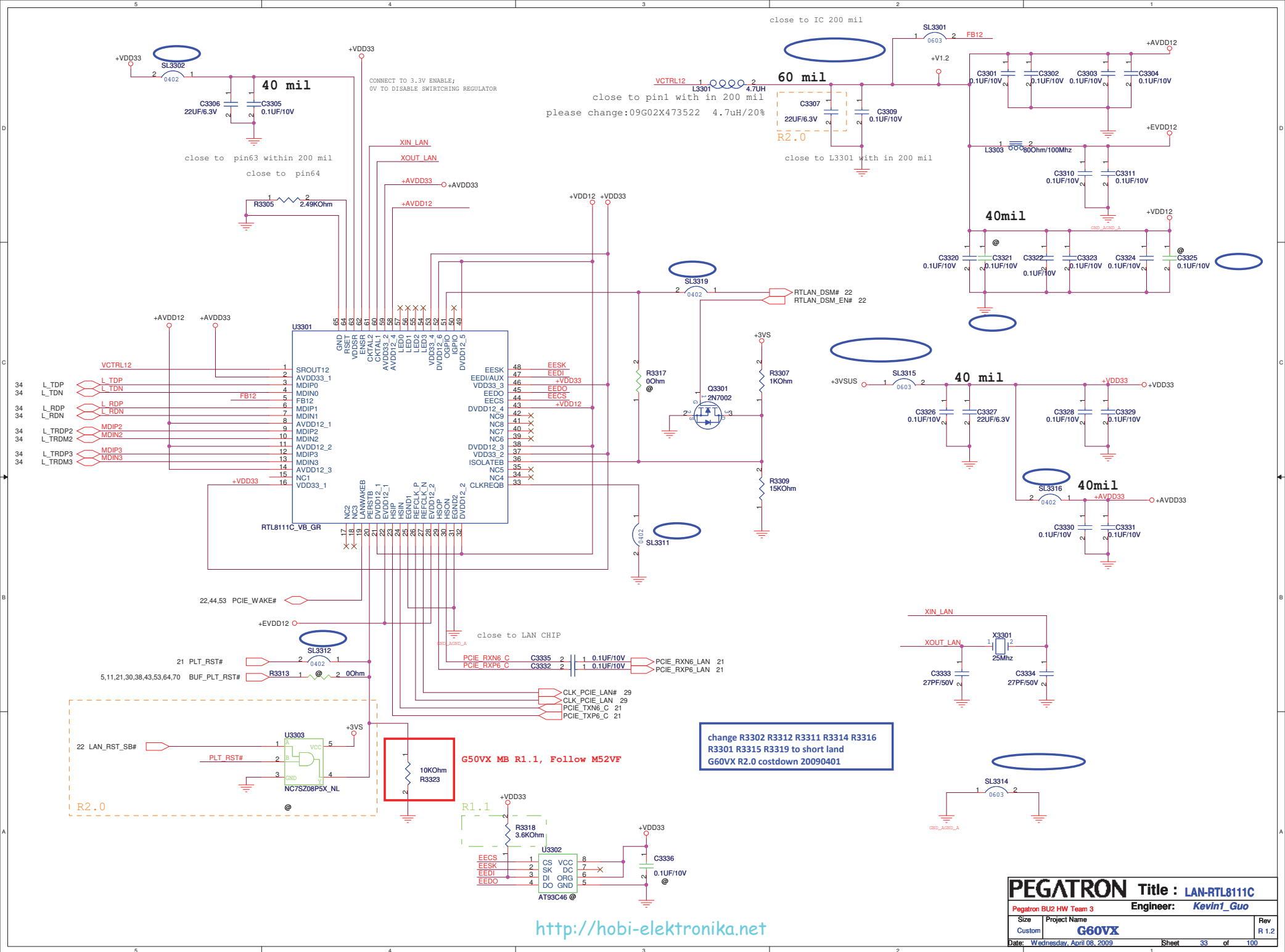
```

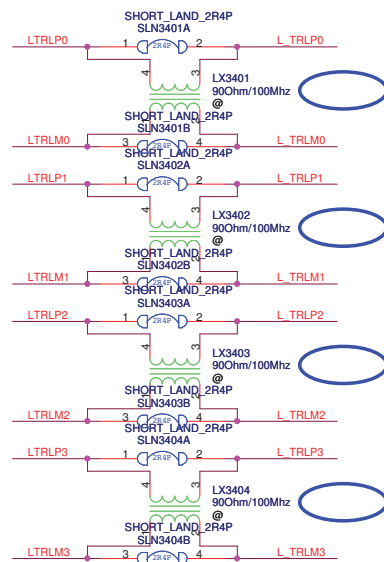
unmount SW3201 D3201 R3201 R3202 R3203 Q3201 Q3202
change R3205 to short land
G60VX R2.0 costdown 20090401

```



Reserve this part for protection  
G60VX R1.2 20090305

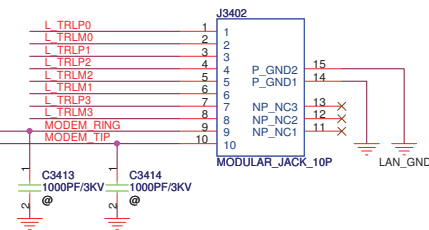
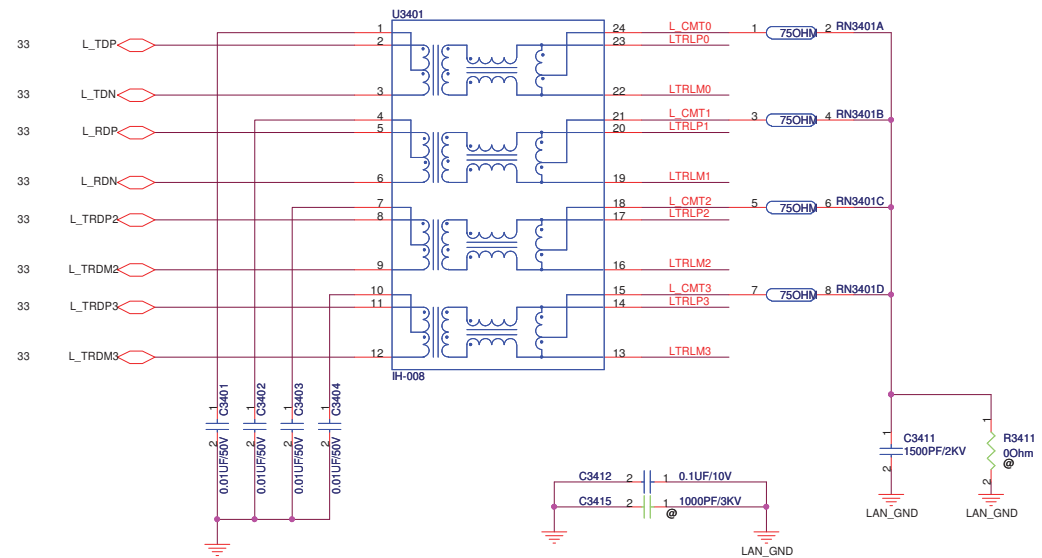


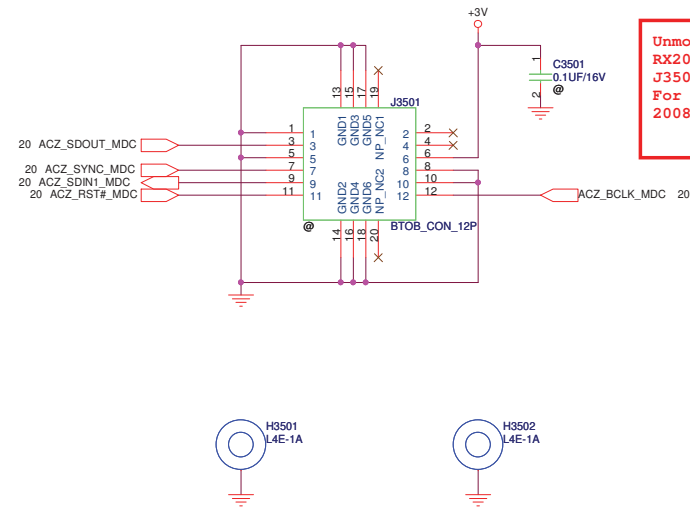


change RNX3401 RNX3402 RNX3403 RNX3404  
to integrated short land;  
change R3409 R3410 to short land  
G60VX R2.0 costdown 20090402

J3401  
SIDE2  
2  
1  
SIDE1  
3  
WT0B\_CON\_2P

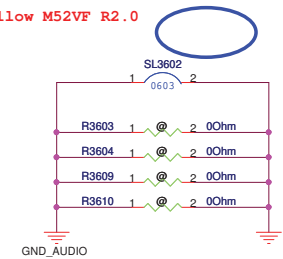
Unmount  
RX2009, RX2012, RX2014, RX2016  
J3501, R3409, R3410, J3401,  
20081107



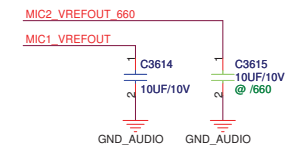
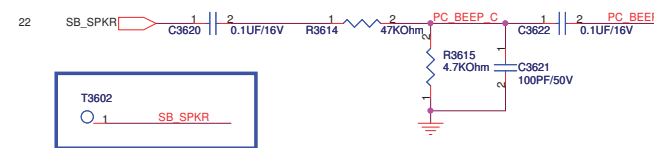


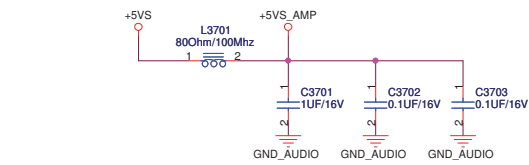
Unmount  
RX2009, RX2012, RX2014, RX2016  
J3501, R3409, R3410, J3401,  
For Modem Delete  
20081107

change R3619 R3621 R3602  
R3624 R3601 R3616 to short land;  
change L3601 to short land;  
unmount C3601 C3605 C3609;  
G60VX R2.0 costdown 20090402

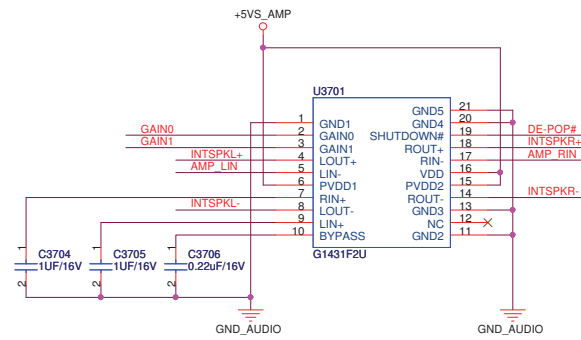


PC BEEP

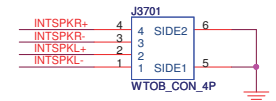




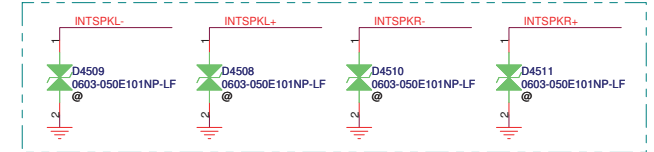
GAIN0	GAIN1	Av (inv)
0	0	6 dB
0	1	10 dB
1	0	15.6 dB
1	1	21.6 dB



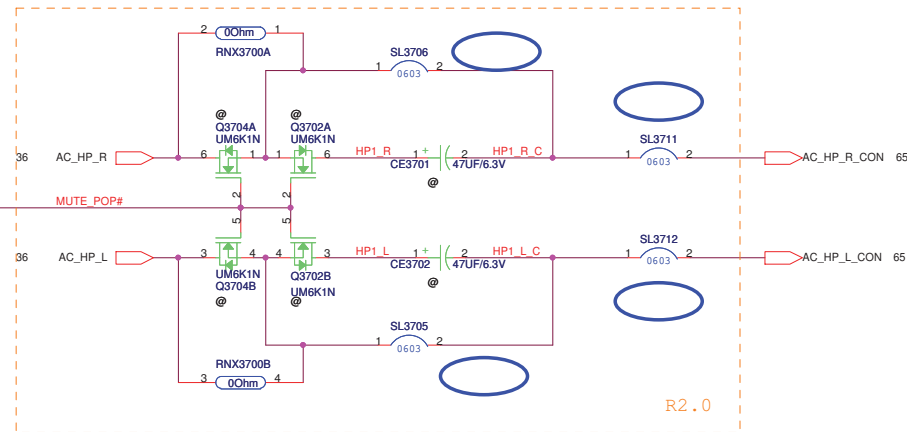
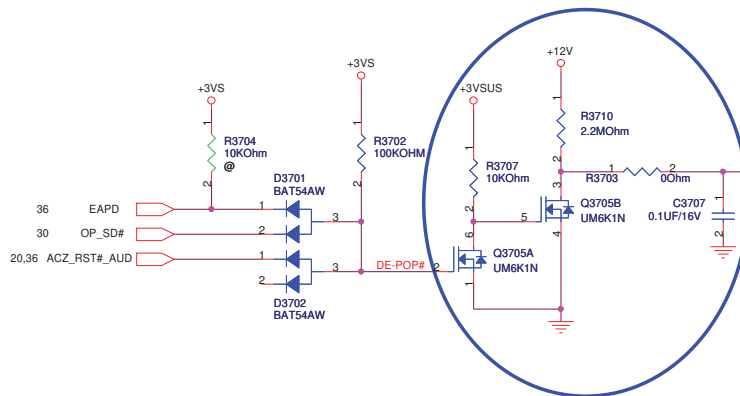
## Internal Speaker Conn.



## Reserved for EMI



R2.0

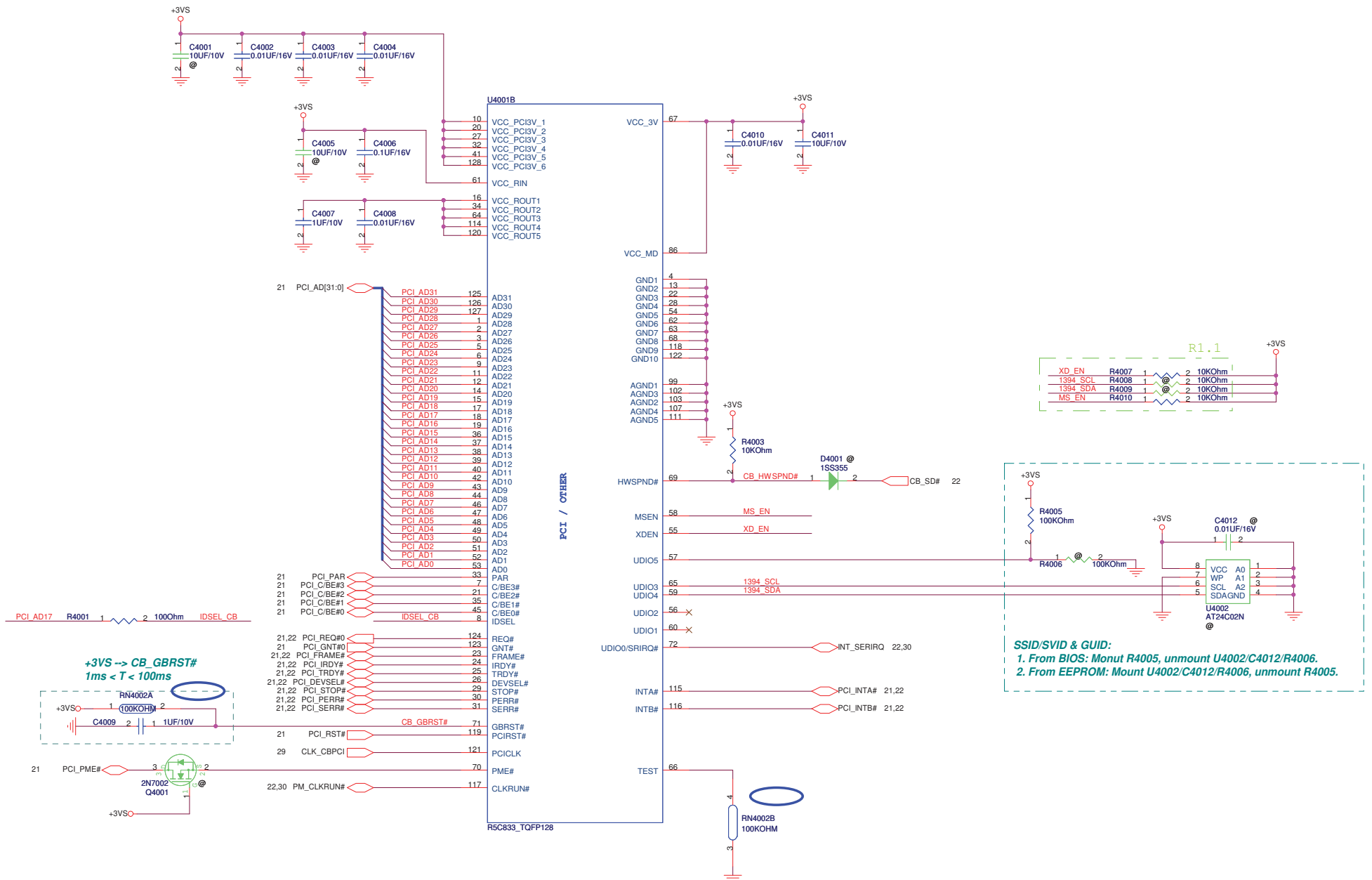


R2.0

unmount R3707 Q3705 R3710 R3703 C3707  
change R3706 R3705 R3711 R3712 to short land  
add SL3700 SL3701  
G60VX R2.0 costdown 20090402

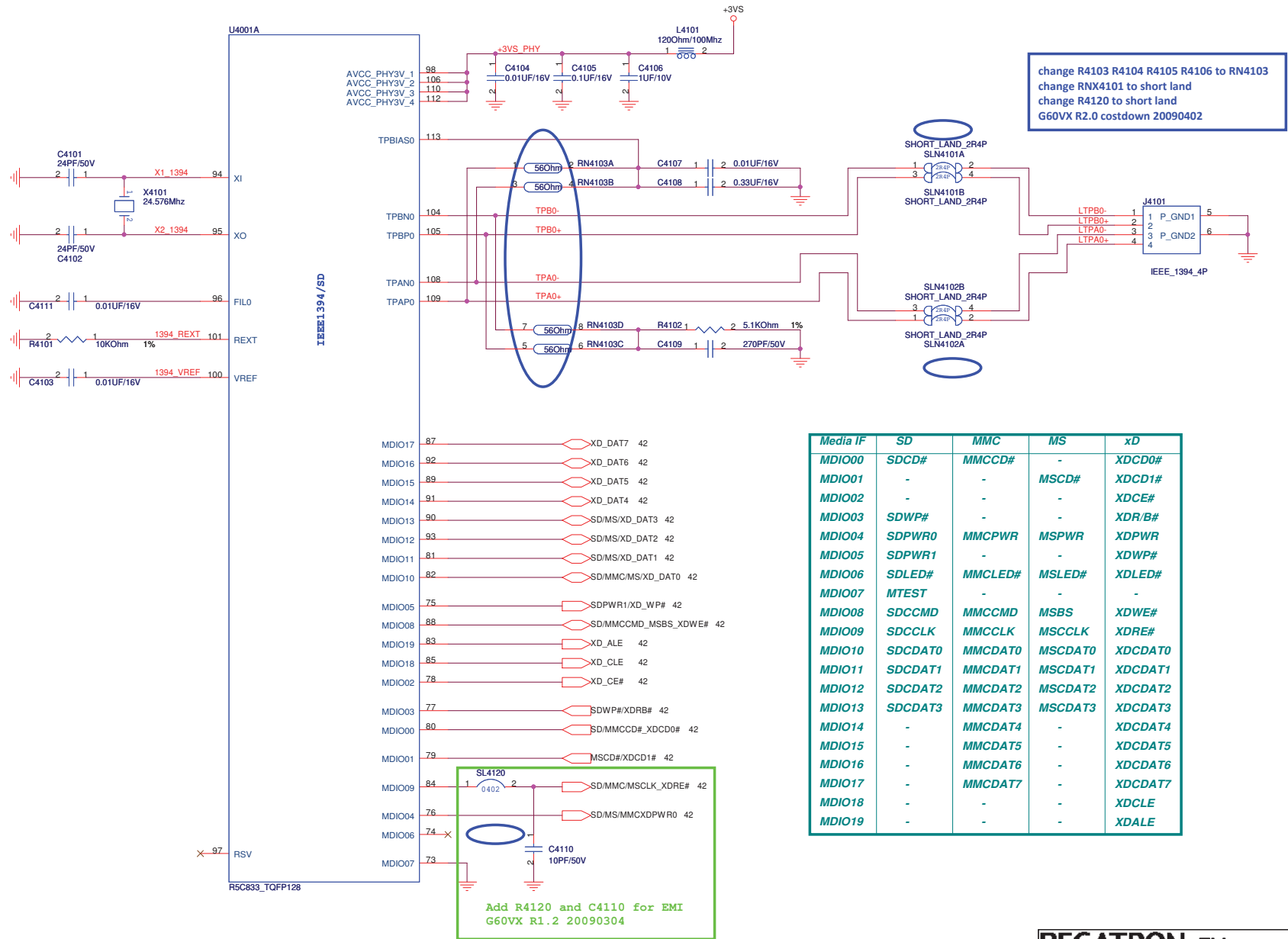


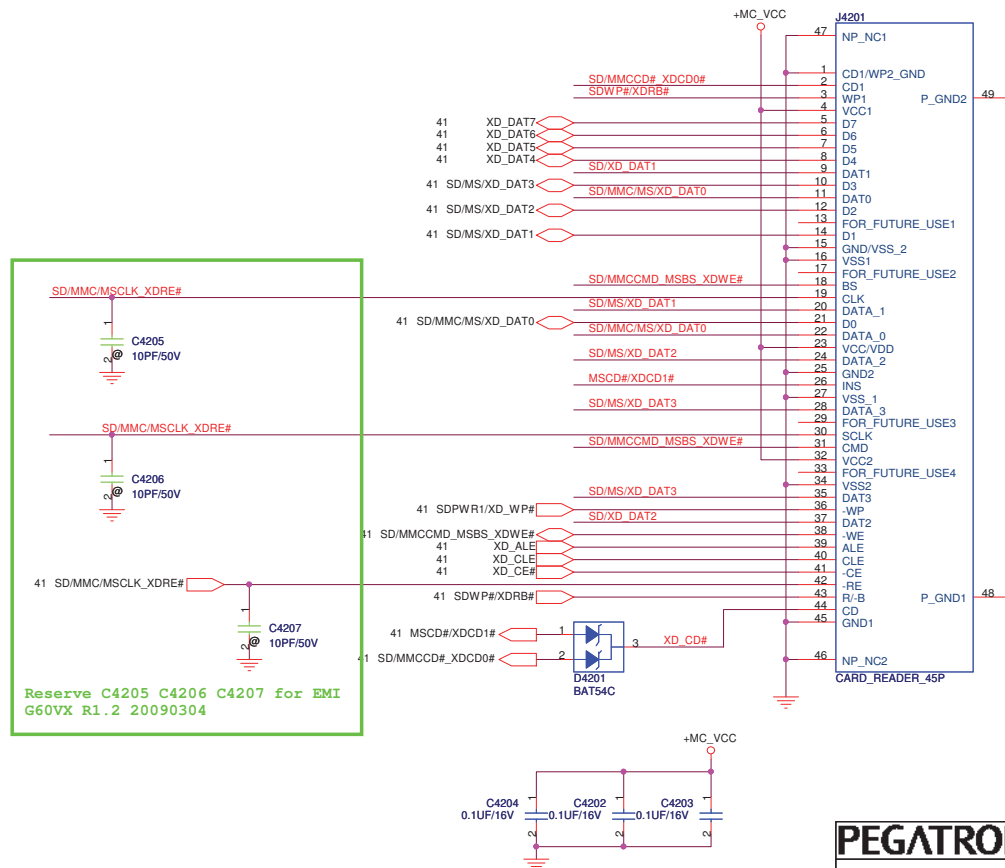
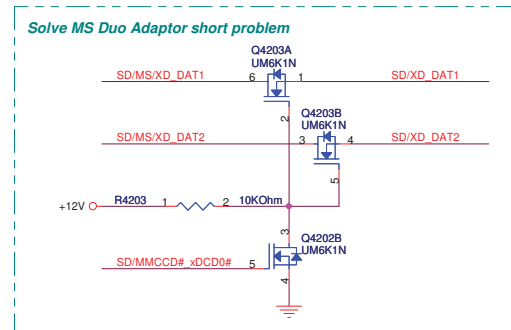
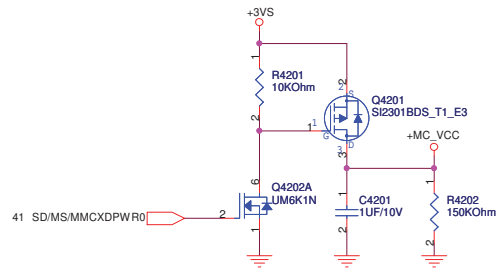




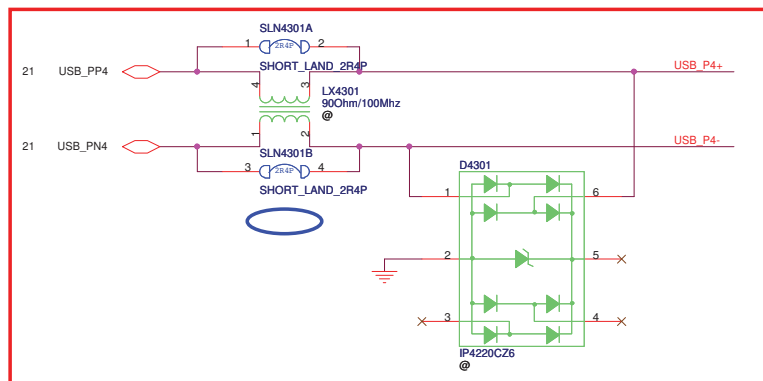
<http://hobi-elektronika.net>

PEGATRON			Title : CB_R5C833	
Pegatron BU2 HW Team 3			Engineer: Kevin1_Guo	
Size	Project Name		Rev	
Custom	G60VX		R 1.2	
Date: Wednesday, April 08, 2009	Sheet		40	of 100

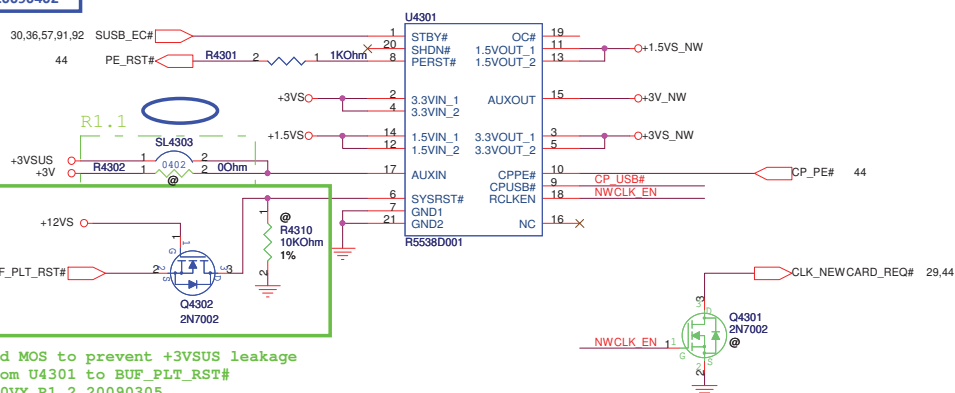




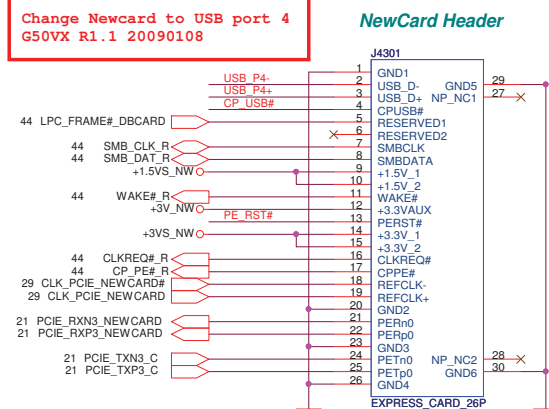
<http://hobi-elektronika.net>



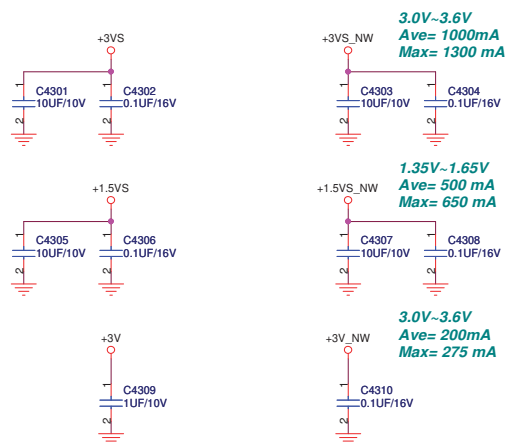
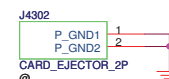
change RNX4301 to short land  
chang R4303 to short land  
G60VX R2.0 costdown 20090402



Add MOS to prevent +3VSUS leakage  
from U4301 to BUF\_PLT\_RST#  
G60VX R1.2 20090305

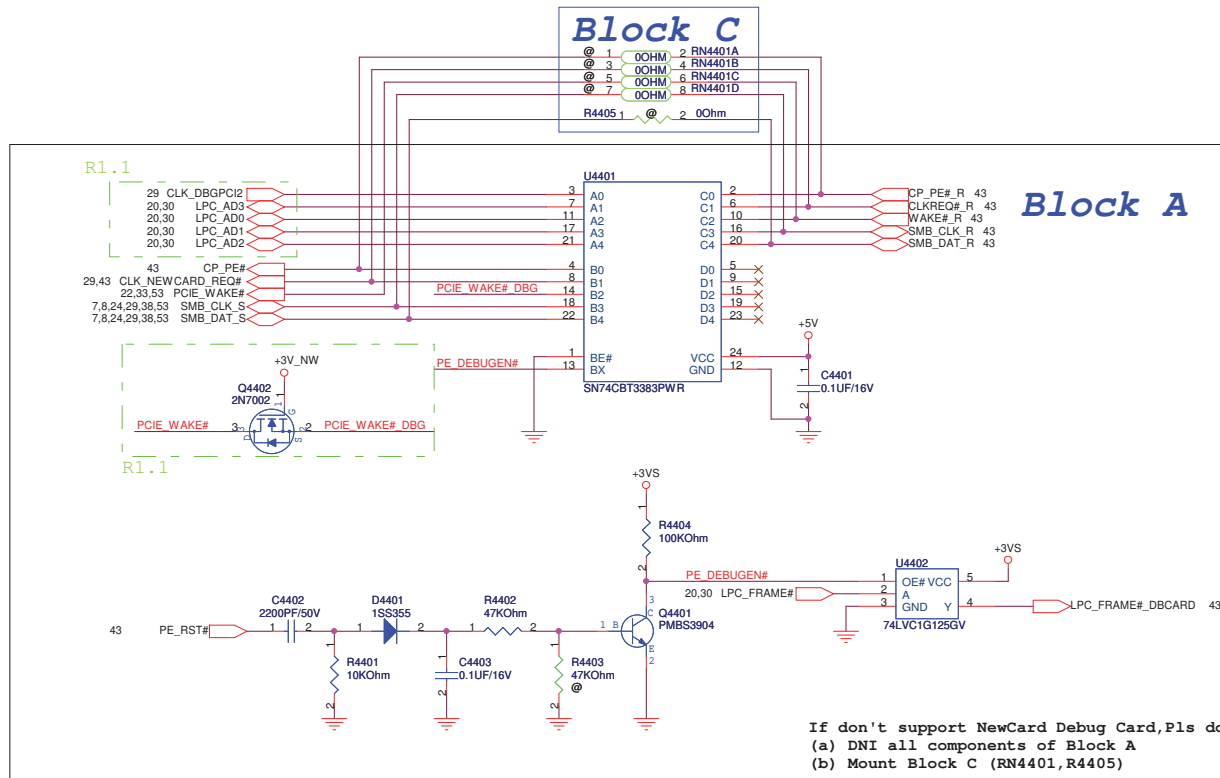


### NewCard Header

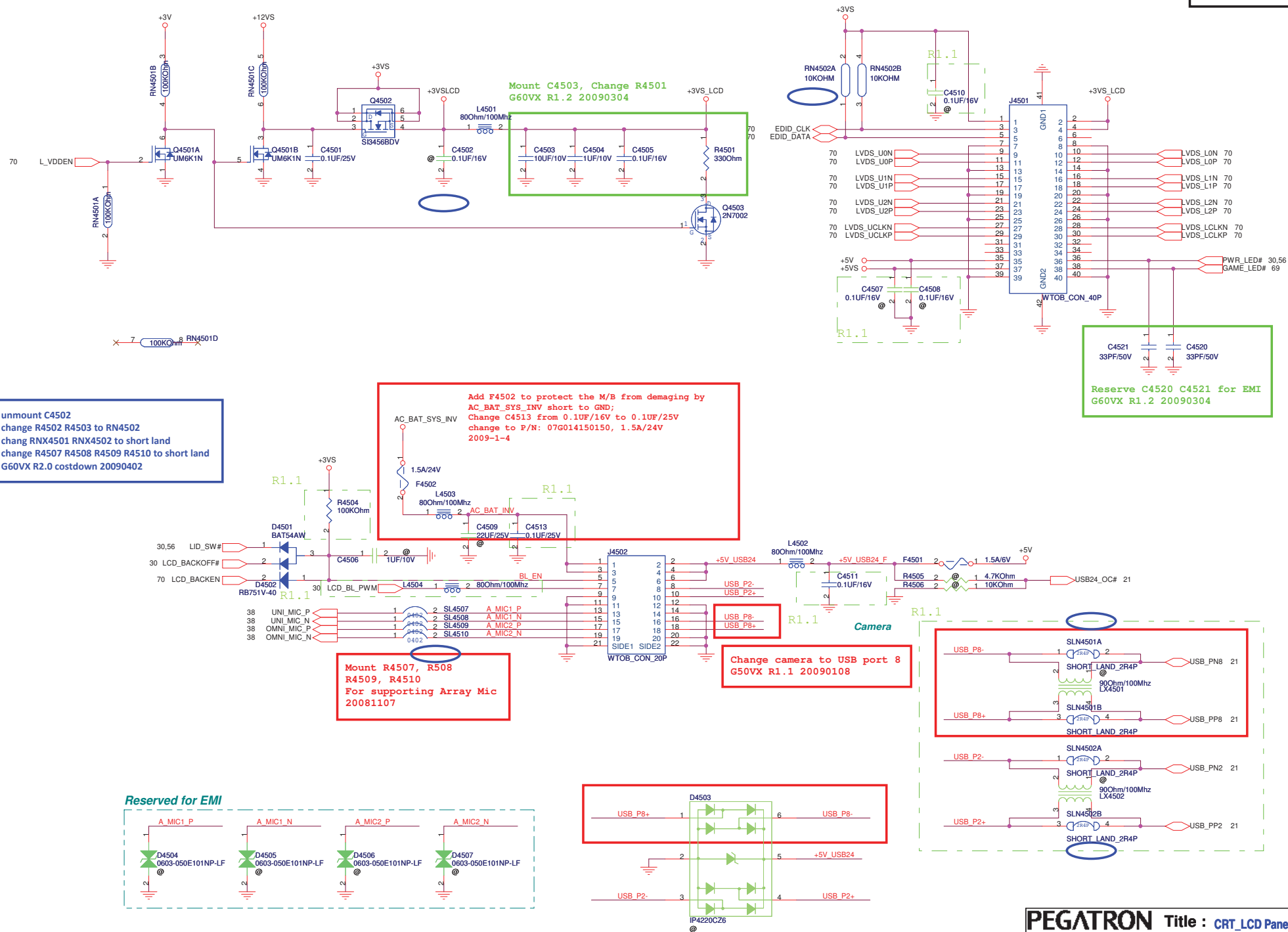


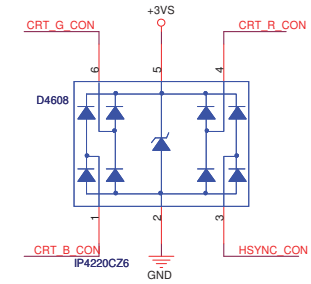
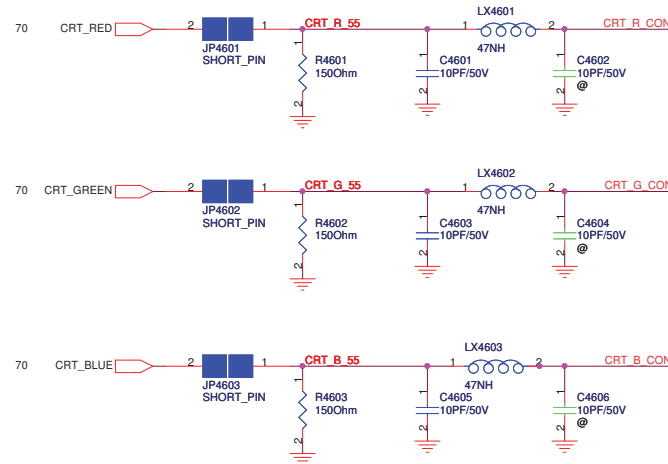
## For NewCard Debug Card

## LPC Debug Port

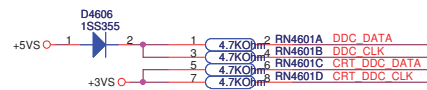
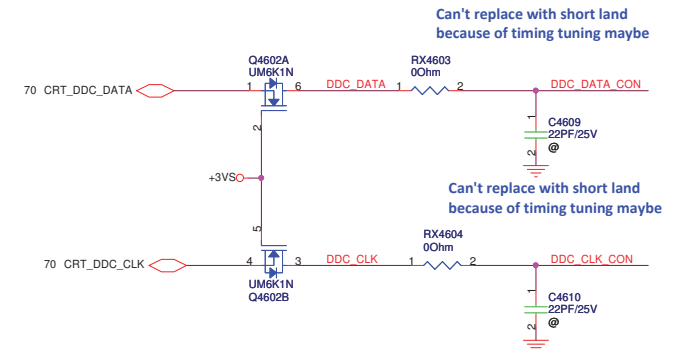
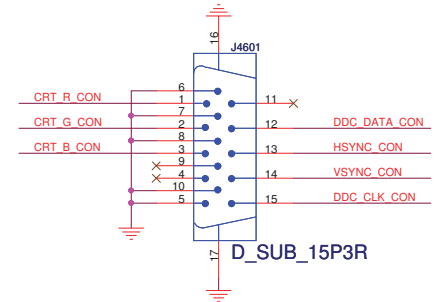
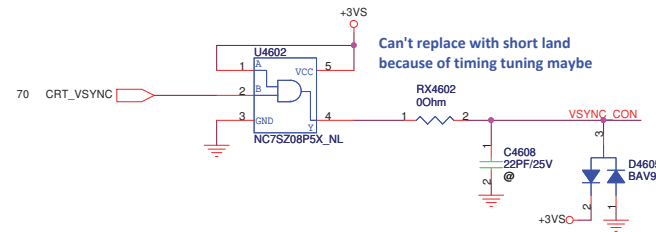
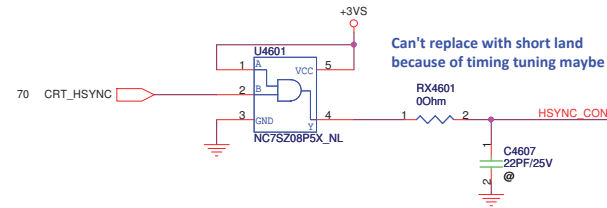


Mount Block A and LPC Debug Port in early stage  
200811170917





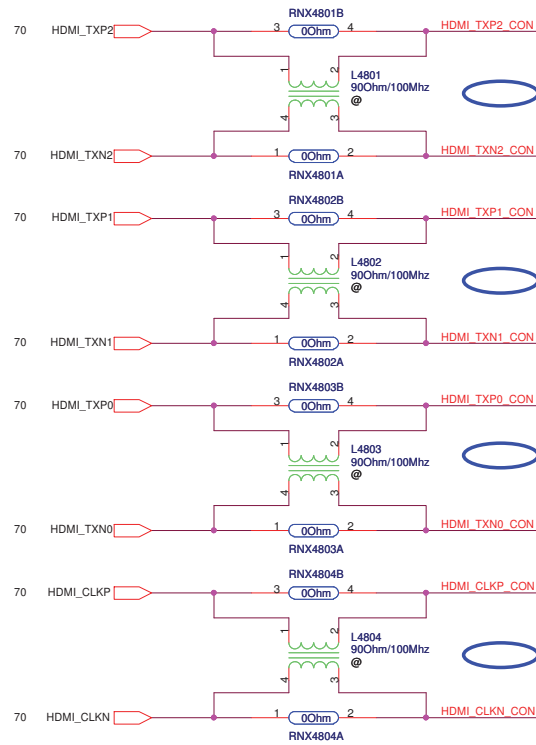
delete RX4605 RX4606 RX4607  
delete D4601 D4602 D4603 D4604  
add D4608  
change RN4601 to 4R8P  
delete RN4602  
G60VX R2.0 costdown 20090402



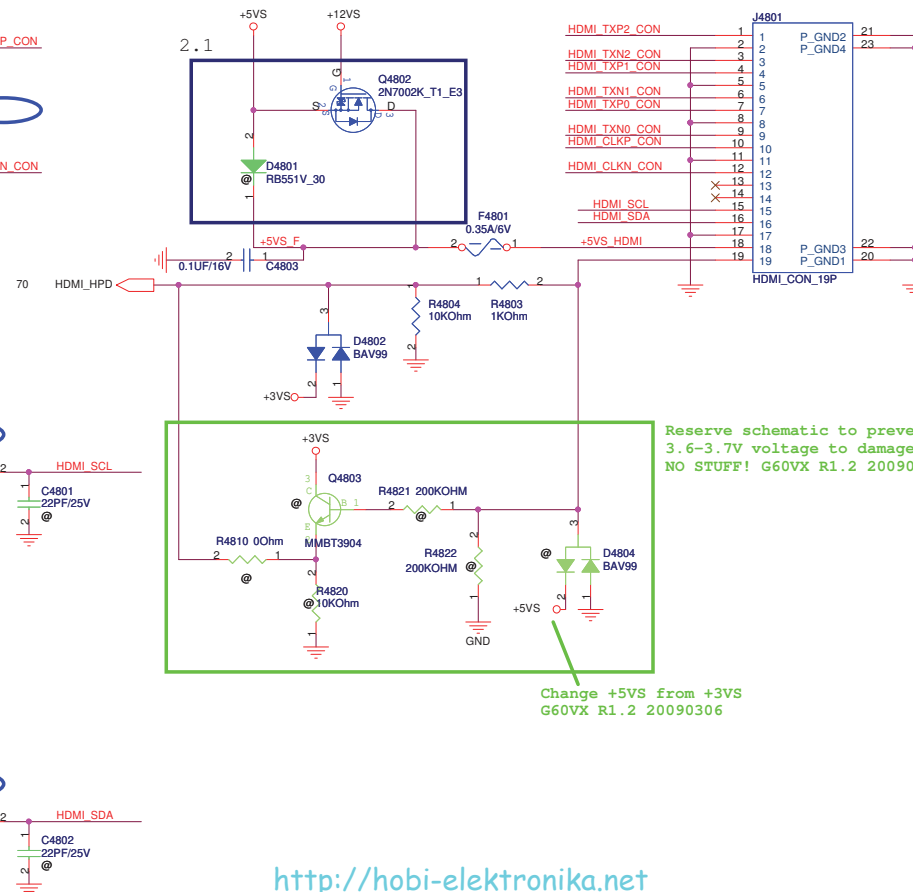
<http://hobi-elektronika.net>

PEGATRON			Title : CRT_D-Sub	
Pegatron BU2 HW Team 3			Engineer: Kevin1_Guo	
Size	Project Name		Rev	
Custom	G60VX		R 1.2	
Date: Thursday, April 02, 2009	Sheet		46	of 100





Reserve RNX4801 RNX4802 RNX4803 RNX4804  
delete RX4809 RX4810 / use short land;  
delete R4801 R4802 / add RN4801  
G60VX R2.0 costdown 20090402

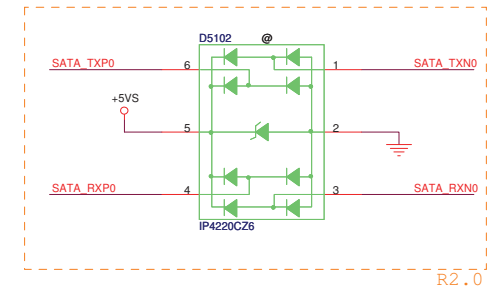
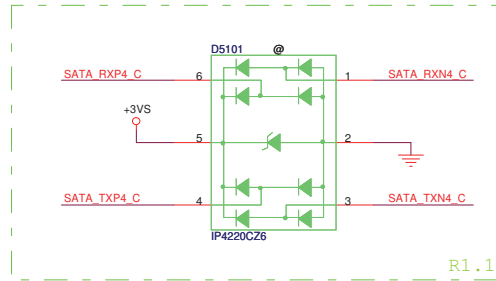
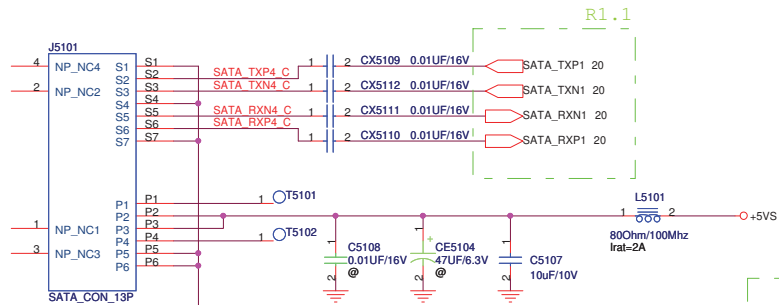


<http://hobi-elektronika.net>

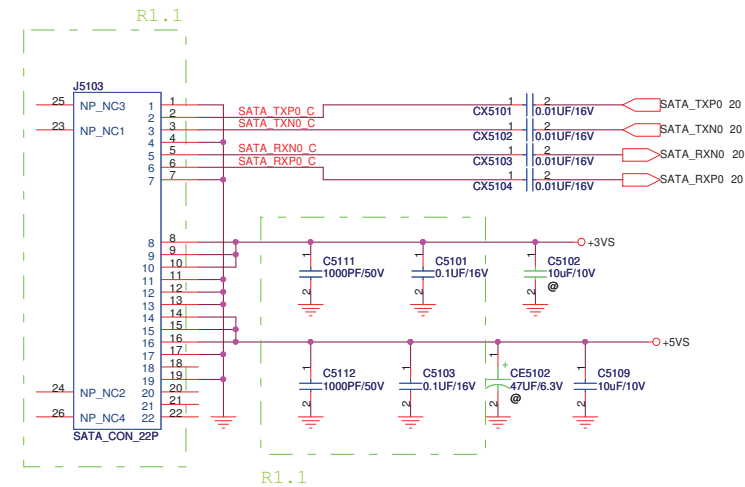
PEGATRON		Title : TV HDMI	
Pegatron BU2 HW Team 3		Engineer: Kevin1_Guo	
Size	Project Name	Rev	
Custom	G60VX	R 1.2	
Date: Wednesday, April 08, 2009	Sheet	48	of 100



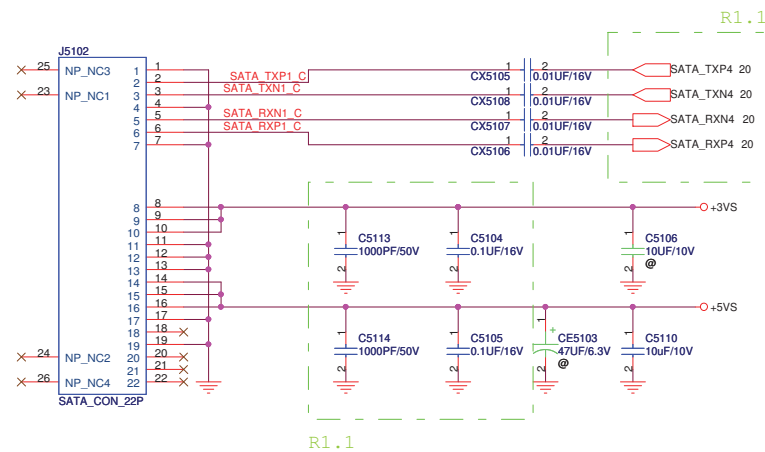
ODD



HDD

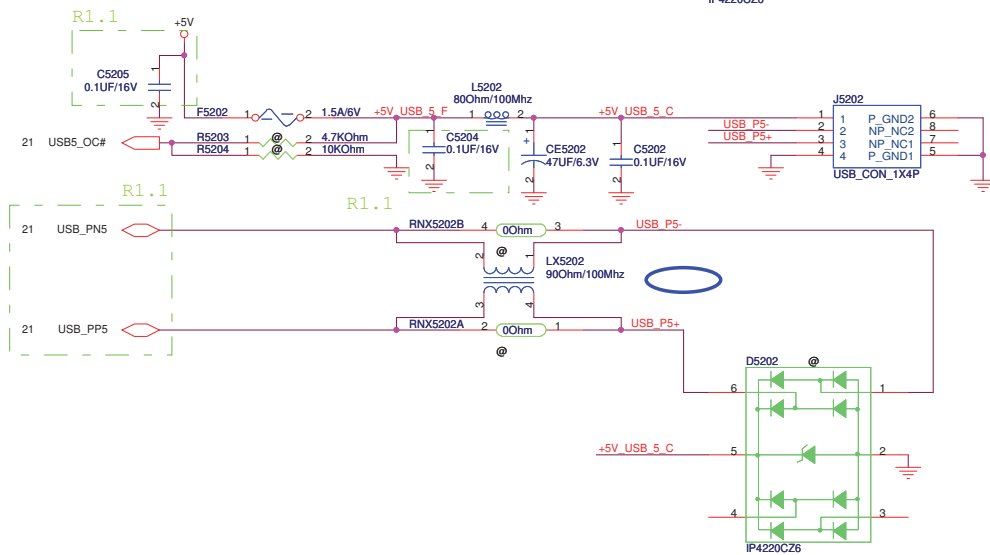
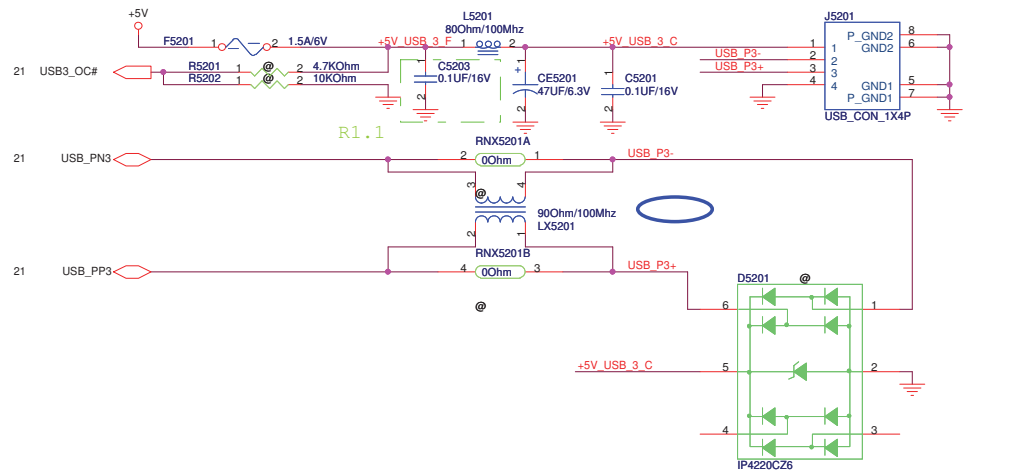


mount CE5102 C5103, unmount C5111  
C5101 C5112 C5109  
G60VX R2.0 costdown 20090402



mount CE5103 C5105, unmount C5113  
C5104 C5114 C5110  
G60VX R2.0 costdown 20090402

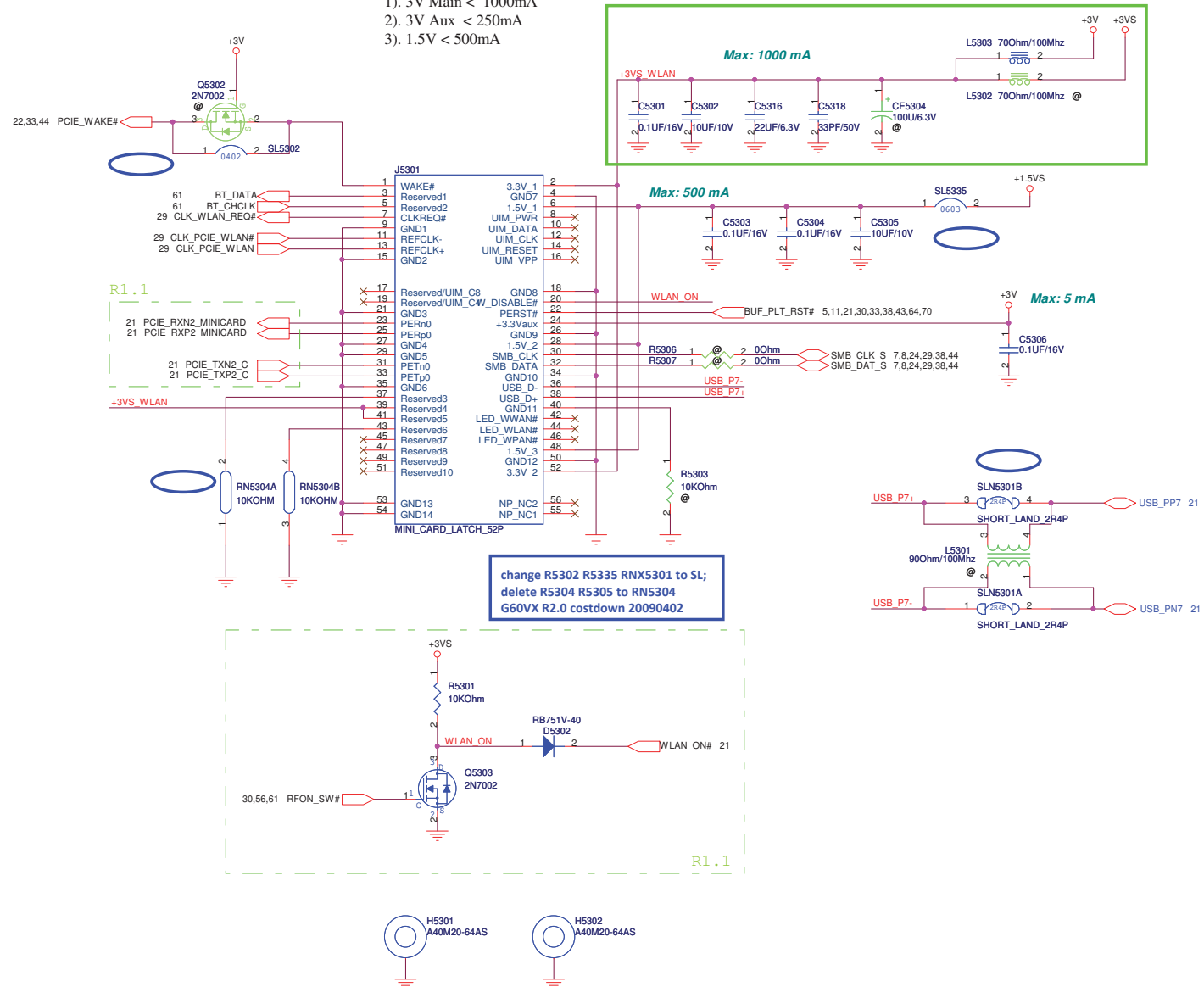
<http://hobi-elektronika.net>

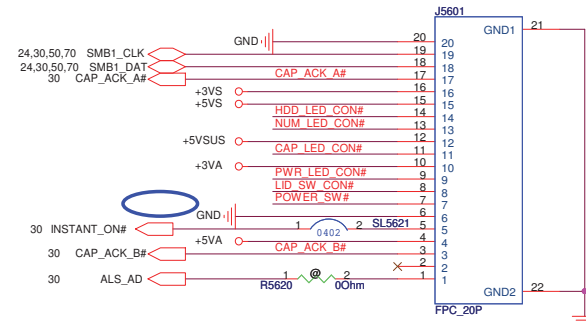
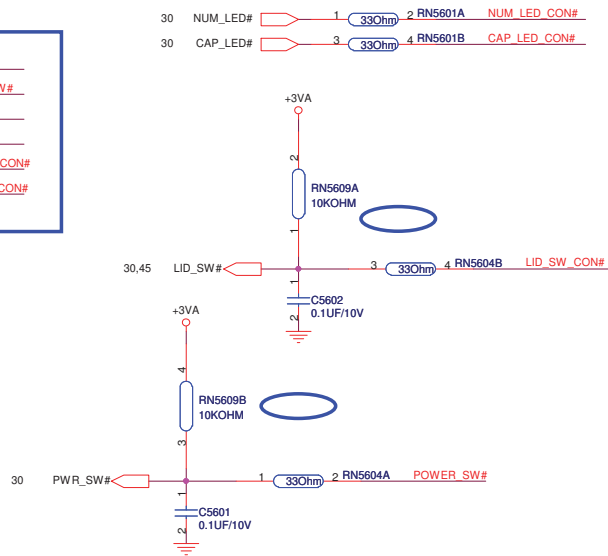
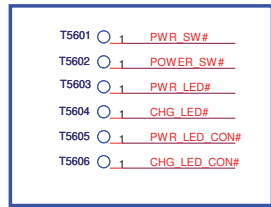


Follow H15HV R2.1 to accommodate large current  
for Intel WiFi link 5300/5100 WLAN card  
G60VX R1.2 20090305

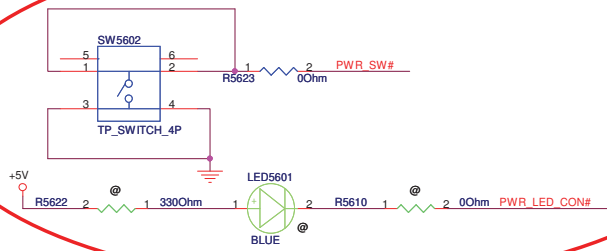
## POWER CONSUMPTION:

- 1). 3V Main < 1000mA
- 2). 3V Aux < 250mA
- 3). 1.5V < 500mA

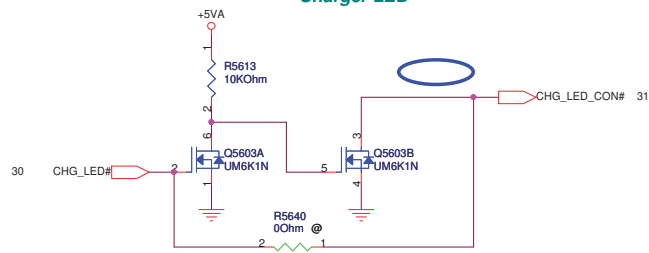




For Test

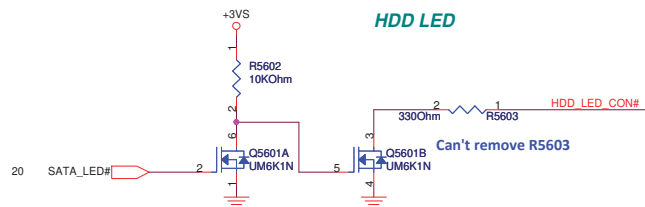


Charger LED

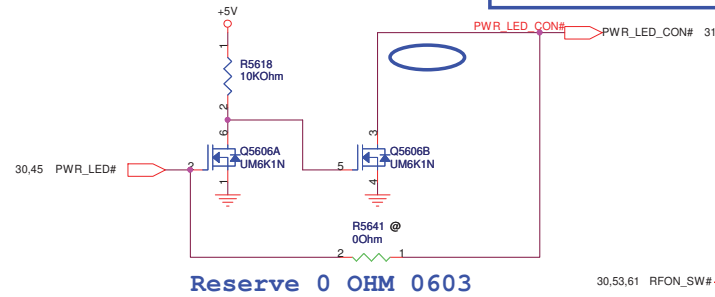


Reserve 0 OHM 0603

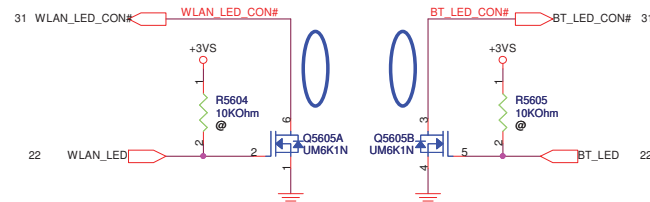
HDD LED



Power LED

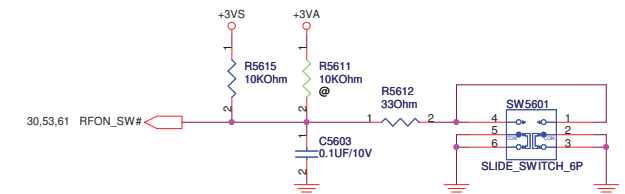


WLAN LED



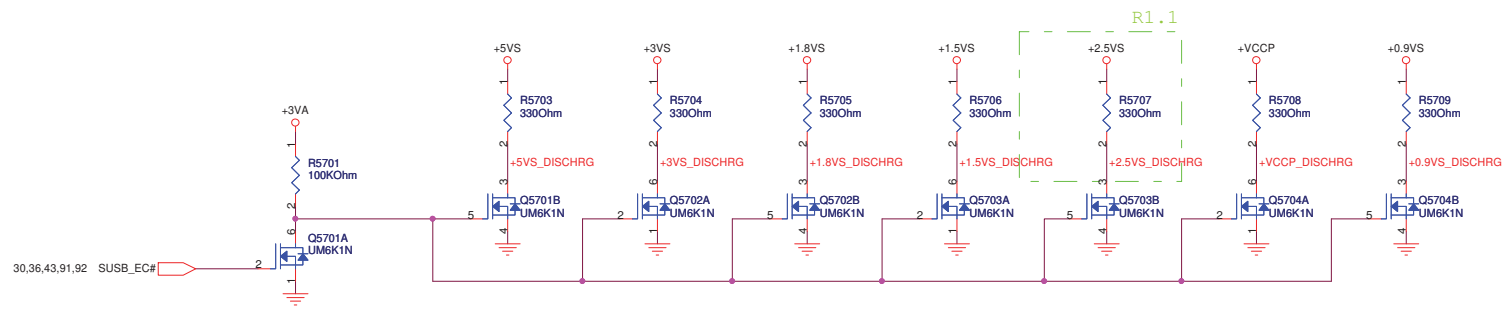
U80V doesn't costdown this MOS

BT LED

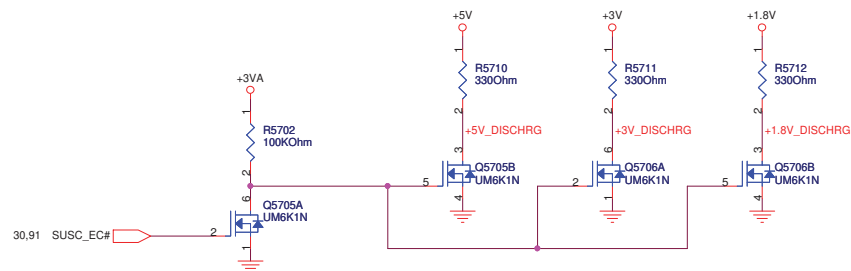


delete R5609 R5607, add RN5609  
 delete R5621  
 delete R5619  
 delete R5614  
 delete R5617 R5616  
 G60VX R2.0 costdown 20090402

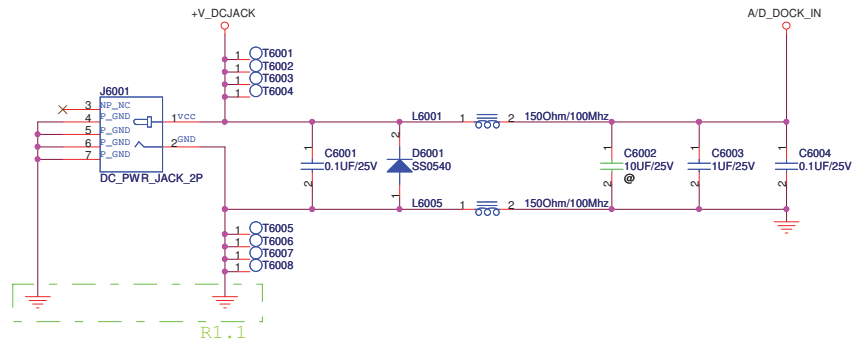
<http://hobi-elektronika.net>



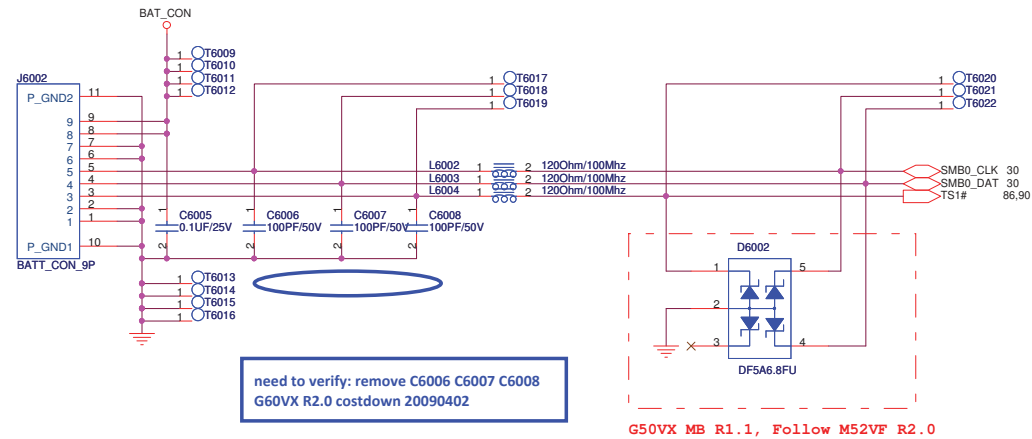
Need to verification!  
G60VX R2.0 costdown 20090402



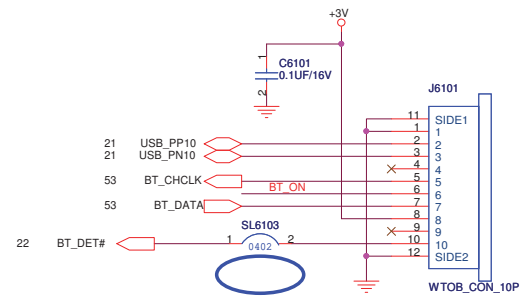
## DC Jack



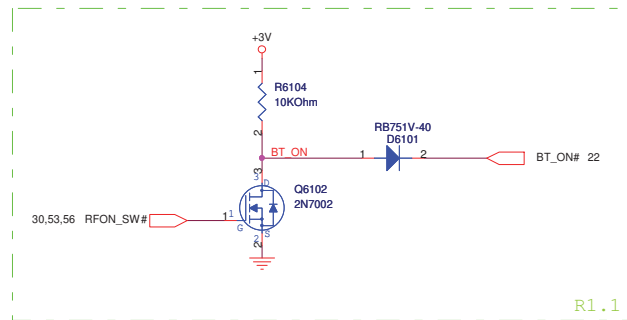
## Battery Connector



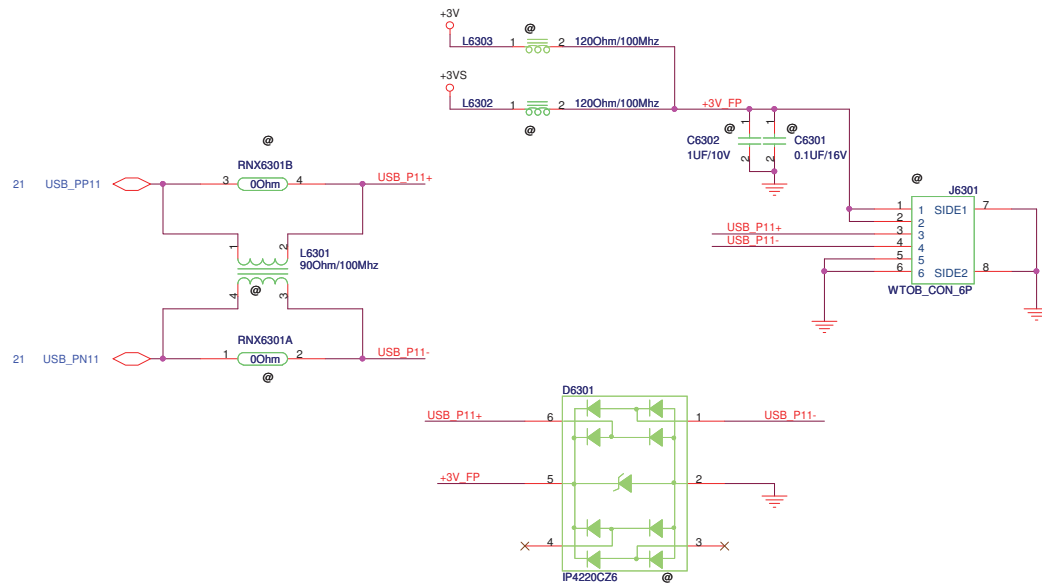




delete R6103  
G60VX R2.0 costdown 20090402

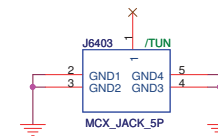
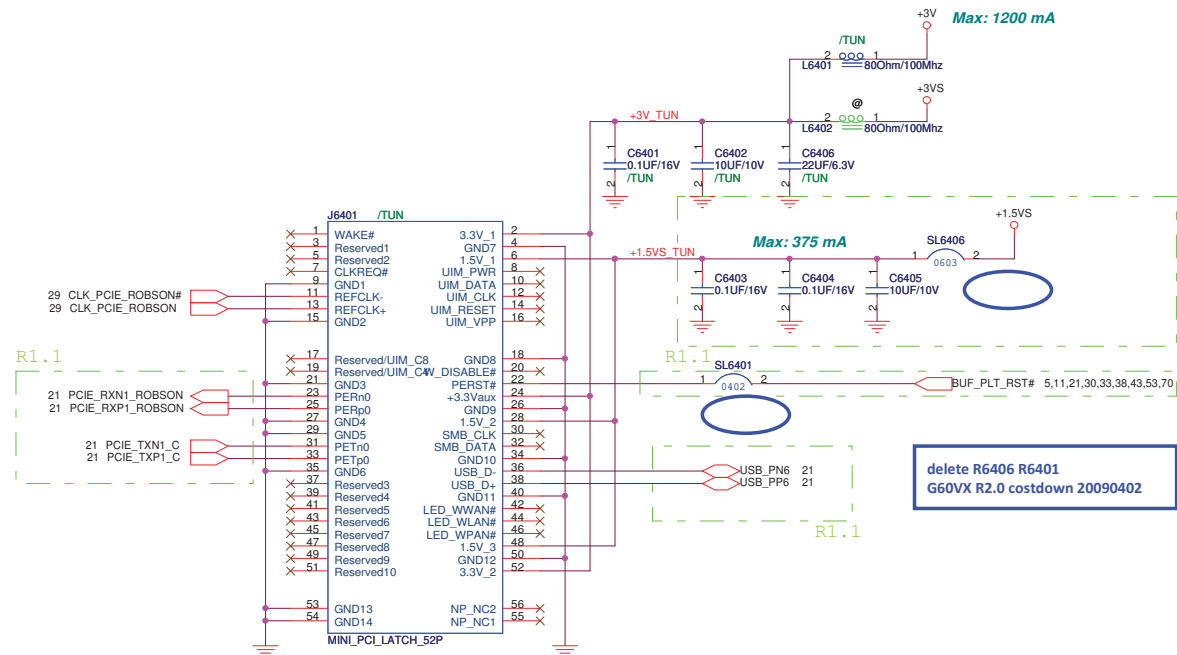


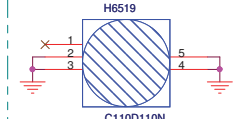
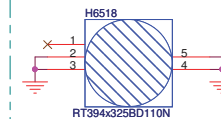
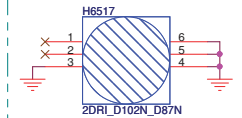
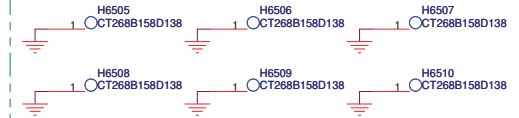
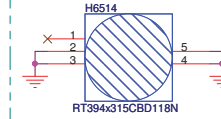
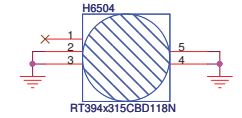
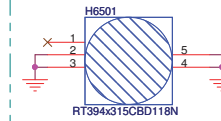
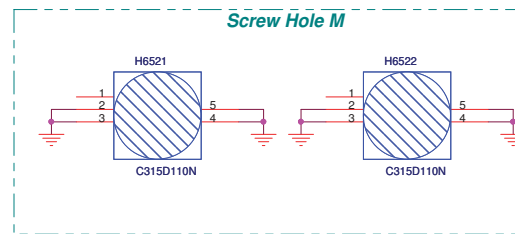
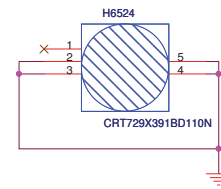
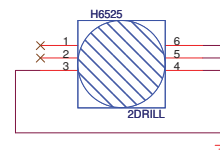
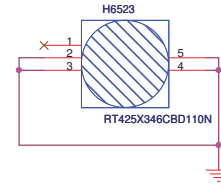
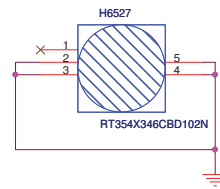
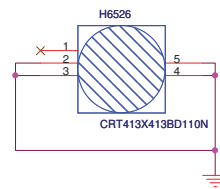
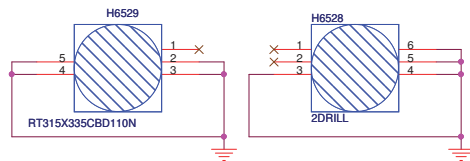
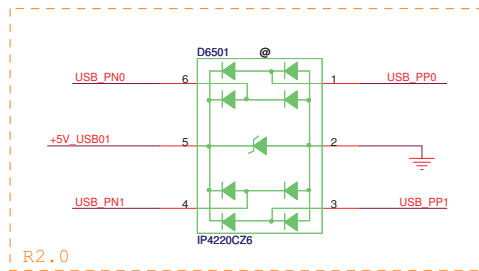
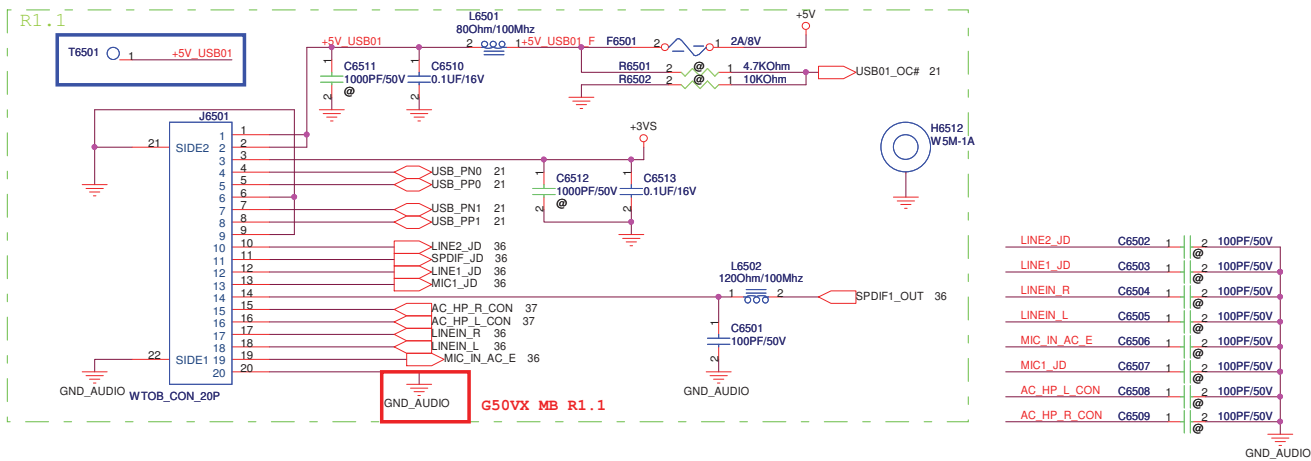
R1.1

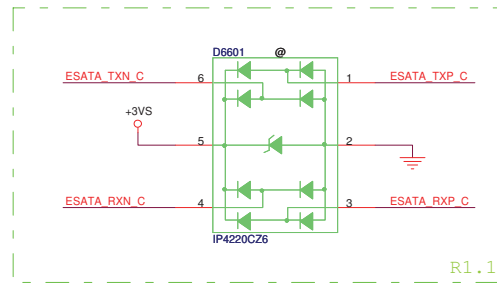
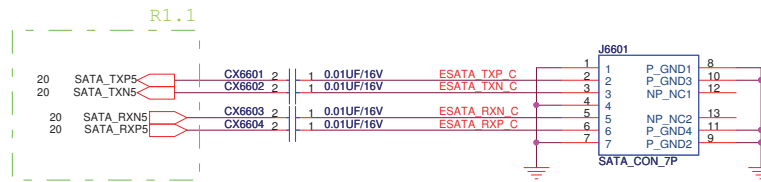


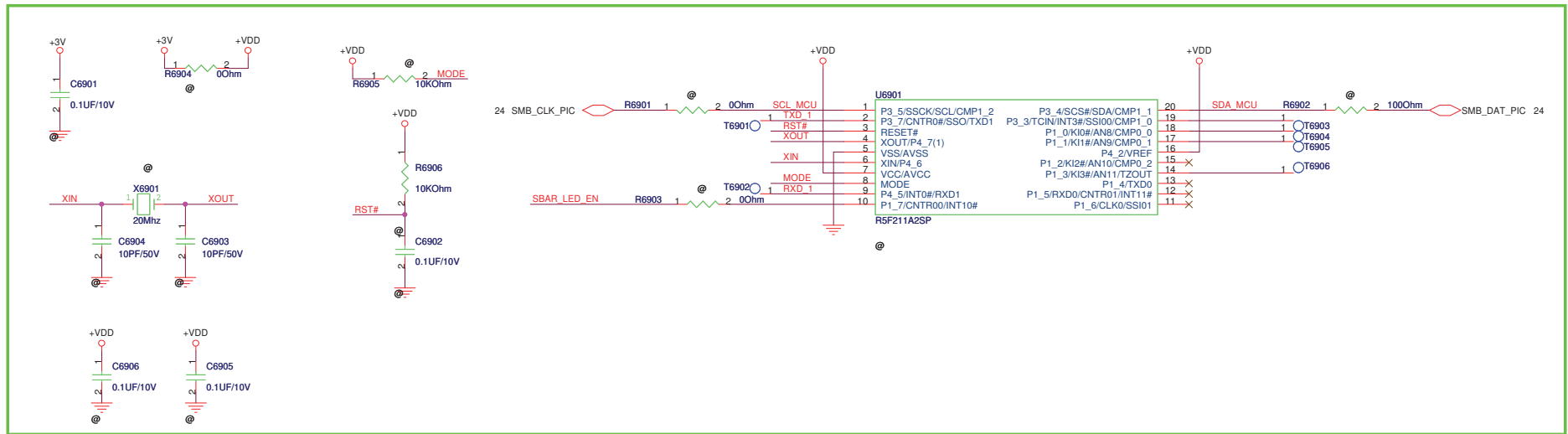
R2.0

Unmount J6301, C6301, C6302, L6302  
 RNx6301 for delete FP connector  
 L6303, L6301, D6301 is reserved  
 200811102025



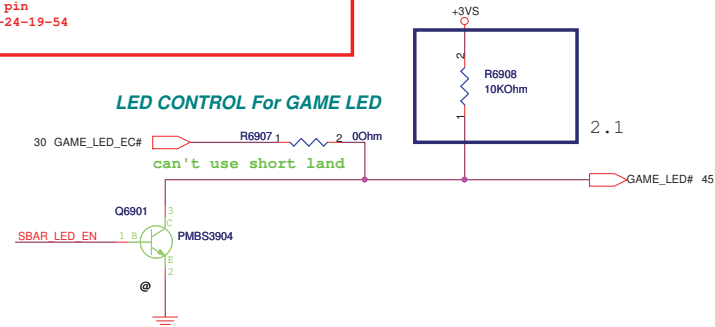






Cause EC will control GAME\_LED#  
Mount R6907 R6908, unmount  
all others and Q2402 RN2402  
G60VX R1.2 20090305

G50VX V1.0, Change net GAME\_LED\_EC# from  
connecting with EC.GPA3 pin to connecting with  
EC.GPA6 pin  
2008-11-24-19-54



AC\_BAT\_SYS

JP7001

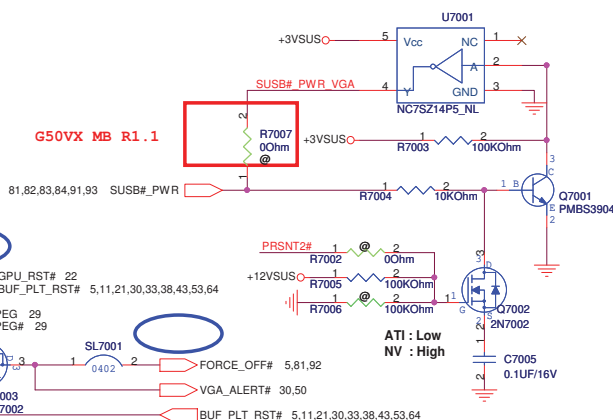
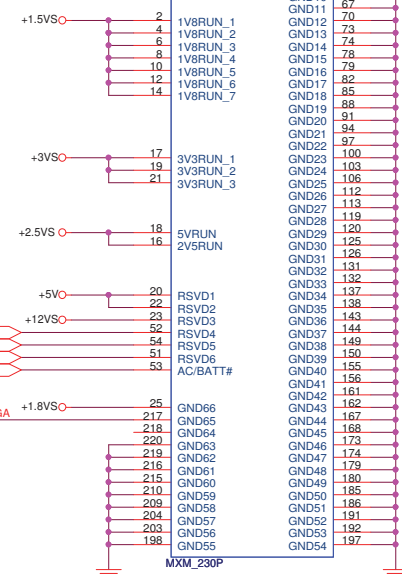
1 2 3

3MM\_OPEN\_5MIL

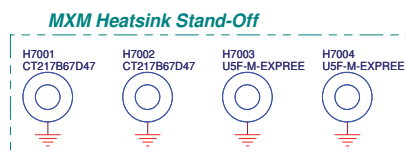
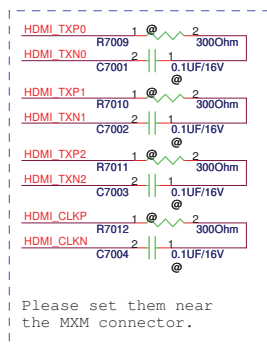
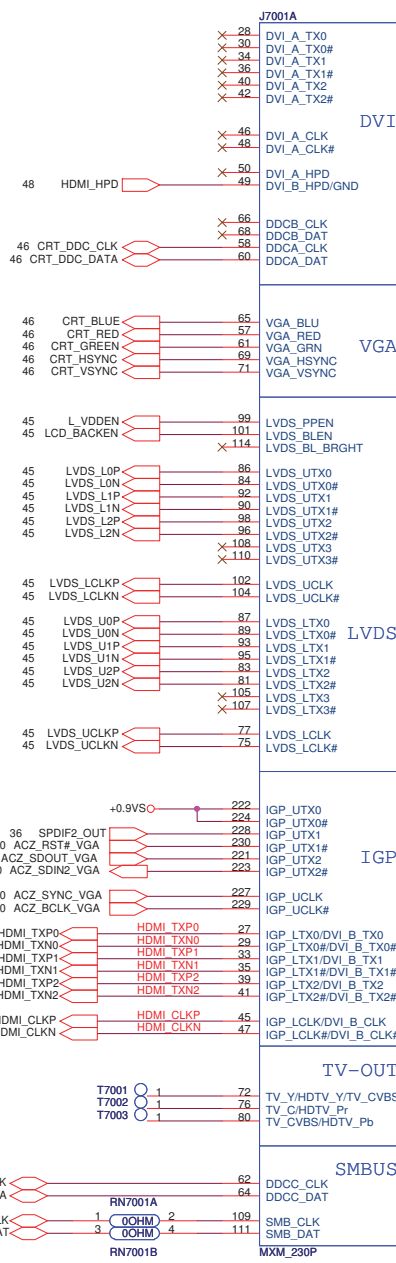
JP7002

1 2 3

3MM\_OPEN\_5MIL

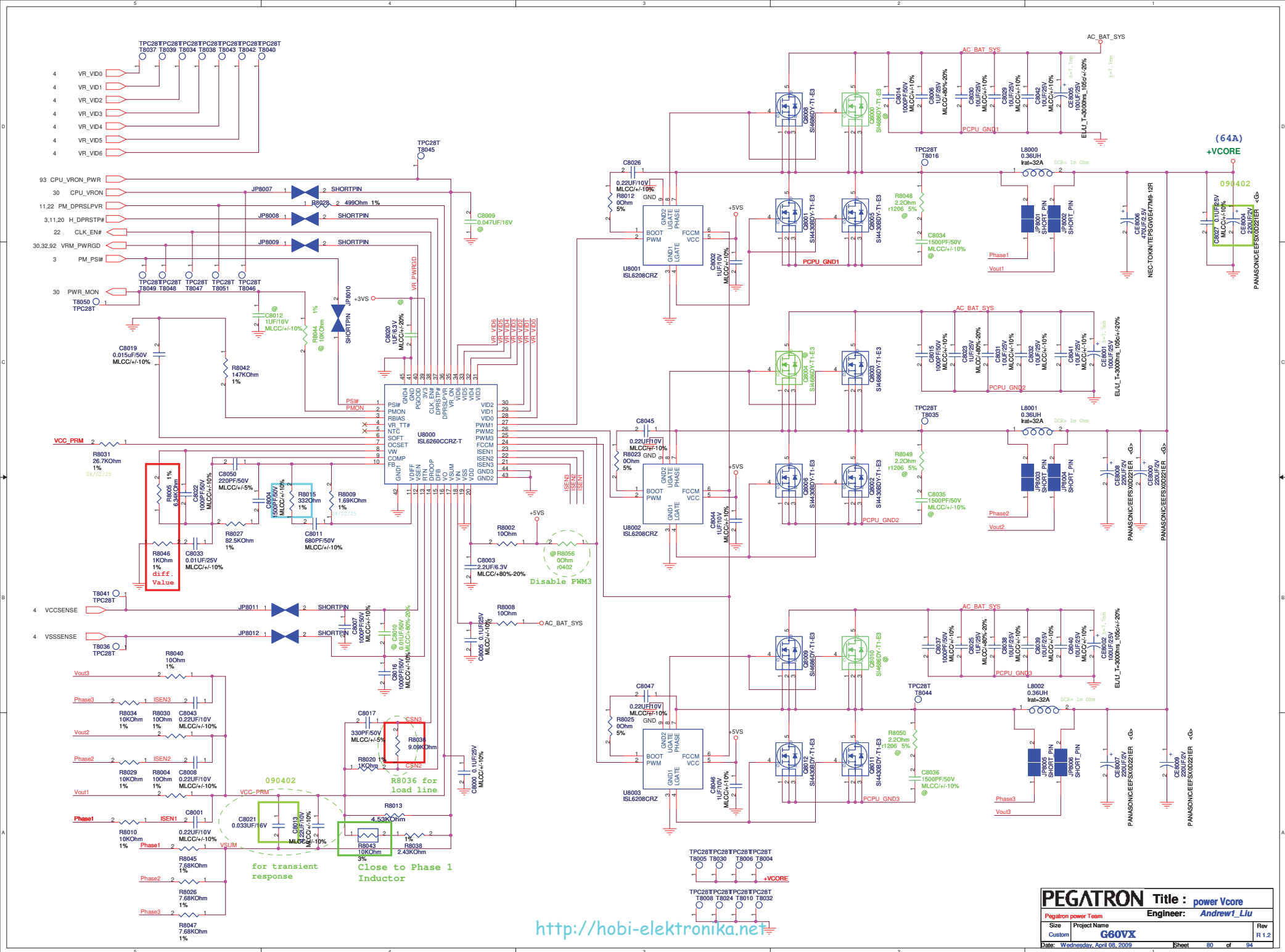


<b>PEGATRON</b>		<b>Title :</b> <u>VGA_MXM</u>	
<b>Pegatron BU2 HW Team 3</b>		<b>Engineer:</b> <u>Kevin1_Guo</u>	
Size Custom	Project Name <b>G60VX</b>	Rev R.1:	
Date: <u>Wednesday, April 08, 2009</u>		Sheet	70 of 100



no change

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+2.5VS



2009/1/13



+1.5VO: ROCSET = R8213 ; R8215 = R8213=10KOhm  
+1.05VO: ROCSET = R8212 ; R8212=R8211=10KOhm

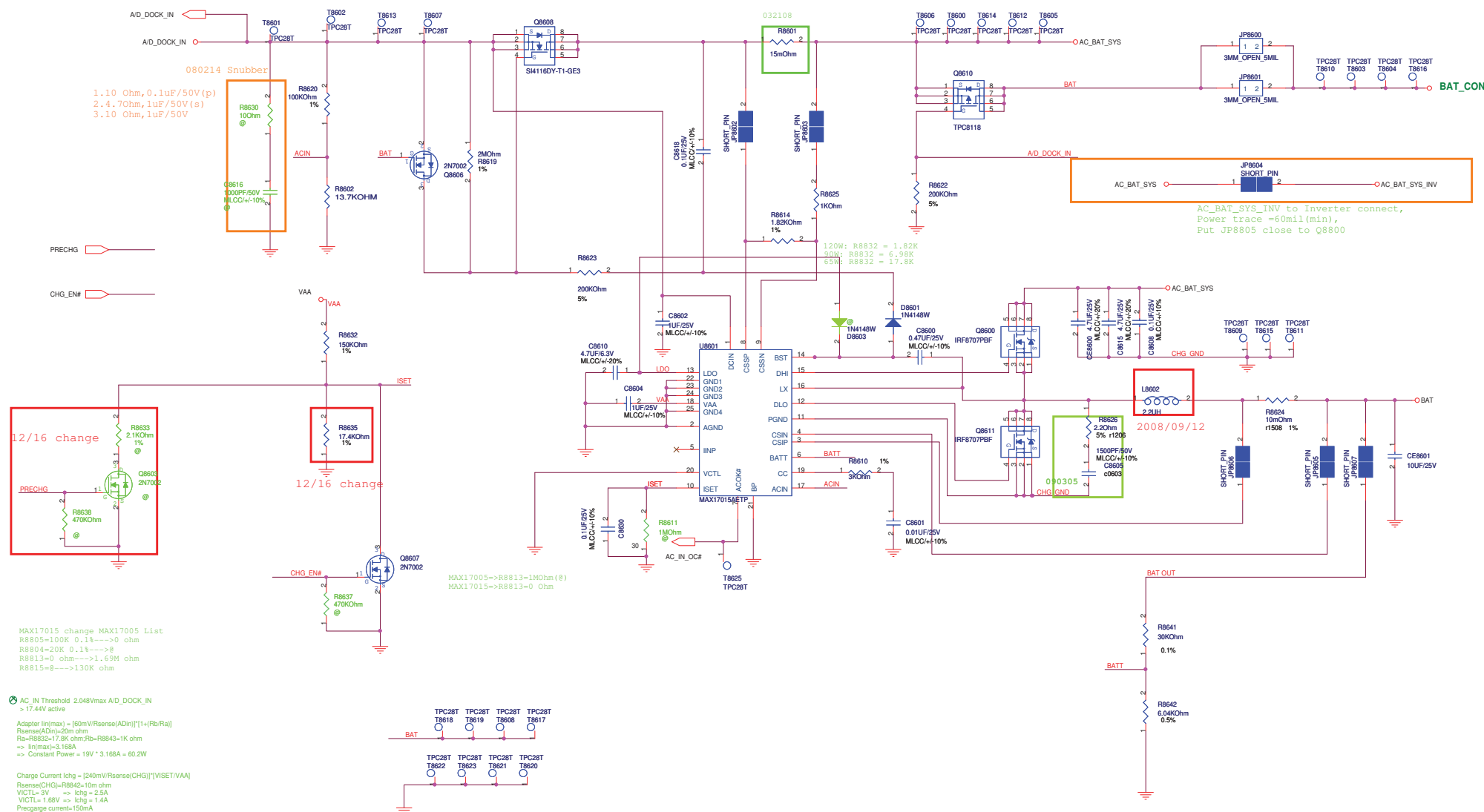
$$\begin{aligned} +1.5\text{V}_O &= V_{\text{REF}} * (R_{8206} + R_{8214}) / R_{8214} = 1.52\text{V} \pm 2.26\% \\ +1.05\text{V}_O &= V_{\text{REF}} * (R_{8207} + R_{8210}) / R_{8207} = 1.052\text{V} \pm 1.9\% \end{aligned}$$

```
+1.5V0: Rfset =R8204; Fsw=360KHz
+1.05V0: Rfset =R8202; Fsw=300KHz
```





## POWER PATH & BAT\_LEARN



```
MAX17005=>R8813=1MOhm(@)
MAX17015=>R8813=0 Ohm
```

```
MAX17015 change MAX17005 List
R8805=100K 0.1%--->0 ohm
R8804=20K 0.1%--->@
R8813=0 ohm--->1.69M ohm
R8815=@--->130K ohm
```

AC\_IN Threshold 2.048Vmax A/D\_DOCK\_IN  
> 17.44V active

```
Adapter lin(max) = [60mV/Rsense(ADin)]*[1+(Rb/Ra)]
Rsense(ADin)=20m ohm
Ra=R8832=17.8K ohm;Rb=R8843=1K ohm
=> lin(max)=3.168A
=> Constant Power = 19V * 3.168A = 60.2W
```

Charge Current Ichg = [240mV/Rsense(CHG)]\*[VISET/VAA]  
Rsense(CHG)=R8842=10m ohm

```
VICTL= 3V      => Ichg = 2.5A
VICTL= 1.68V   => Ichg = 1.4A
Precharge current=150mA
```

2.4V<VCTL<4.2V=>3cell=>Vcell =4.2V+(4.2V-VVCTL)/6  
3 cell=>VCTL= 3.9V => Vcell = 4.635V  
0V<VCTL<1.8V=>4cell=>Vcell =4.2V+(VVCTL/6)  
4 cell=>VCTL= 0.3V => Vcell = 4.635V

Mode pin : Vmode > 2.8V (tie to LDO pin) ----> 4 Cells  
2.0 > Vmode > 1.6V (floating) ----> 3 Cells  
0.8 > Vmode (tie to GND) ----> Learning mode

VICTL < 0.8V or DCIN < 7V -->Charger Disable

VCTL = 3.9V; CHG VOLTAGE = 4.25/CELL(3 CELL)

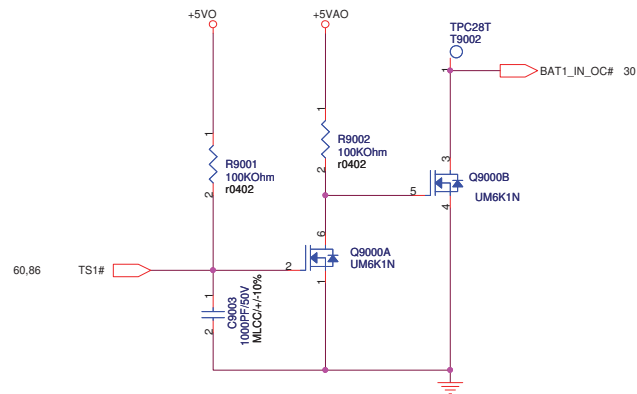
---

5

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<http://hobi-elektronika.net>

# BATTERY IN DETECT



<http://hobi-elektronika.net>

<b>PEGATRON</b>		Title : <b>POWER_DETECT</b>	
Pegatron power Team		Engineer: <b>Andrew1_Liu</b>	
Size Custom	Project Name <b>G60VX</b>		Rev R 1.2
Date: Wednesday, April 08, 2009		Sheet	90 of 94

SUSC#\_PWR POWER

92 SUSB\_EC#

82,83,93 SUSB#\_PWR

TPC26T T9131

TPC26T T9135

R9105

1

2 SHORTPIN

SUSC\_EC#

83,93 SUSC#\_PWR

TPC26T T9121

TPC26T T9134

R9104

1

2 SHORTPIN

<Variant Name>

PEGATRON

Title :POWER\_LOAD SWITCH

Engineer: Andrew1\_Liu

Size

Project Name

Custom

G60Vx

Date: Wednesday, April 08, 2009

Sheet 91 of 94

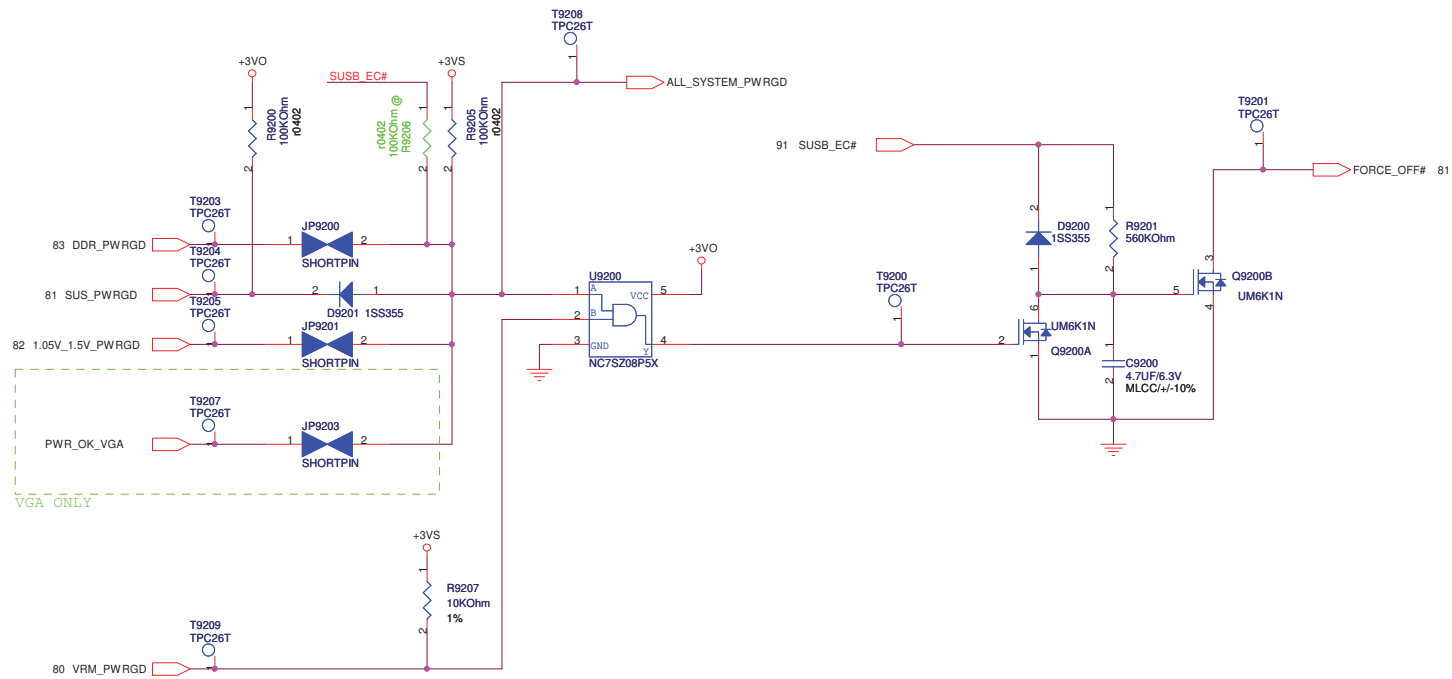
Rev 1.2

elektronika.net

2

1

# POWER GOOD DETECTOR



<http://hobi-elektronika.net>

<Variant Name>		Title :POWER_PROTECT	
Size Custom		Engineer: Andrew1_Liu	
Date: Wednesday, April 08, 2009		Sheet 92 of 94	
Rev 1.2		G60Vx	



AC\_BAT\_SYS ○ → AC\_BAT\_SYS 80,81,82,83,88  
 BAT ○ → BAT 88  
 BAT\_CON ○ → BAT\_CON 88

+3VA ○ → +3VA 81  
 +5VAO ○ → +5VAO 81,90  
 +5VA ○ → +5VA 81

+5VO ○ → +5VO 81,82,83,90,91  
 +3VO ○ → +3VO 81,91  
 +1.8VO ○ → +1.8VO 83  
 +0.9VO ○ → +0.9VO 83  
 +1.05VO ○ → +1.05VO 80,82  
 +1.5VO ○ → +1.5VO 82

+5VSUS ○ → +5VSUS 81  
 +3VSUS ○ → +3VSUS 81,92  
 +12VSUS ○ → +12VSUS 81,91

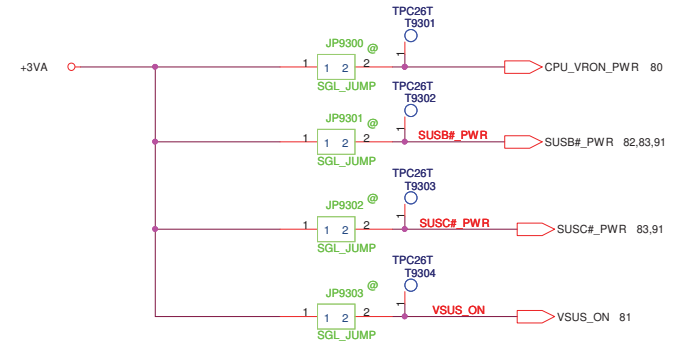
+5V ○ → +5V 91  
 +3V ○ → +3V 91  
 +12V ○ → +12V 91  
 +1.8V ○ → +1.8V 83

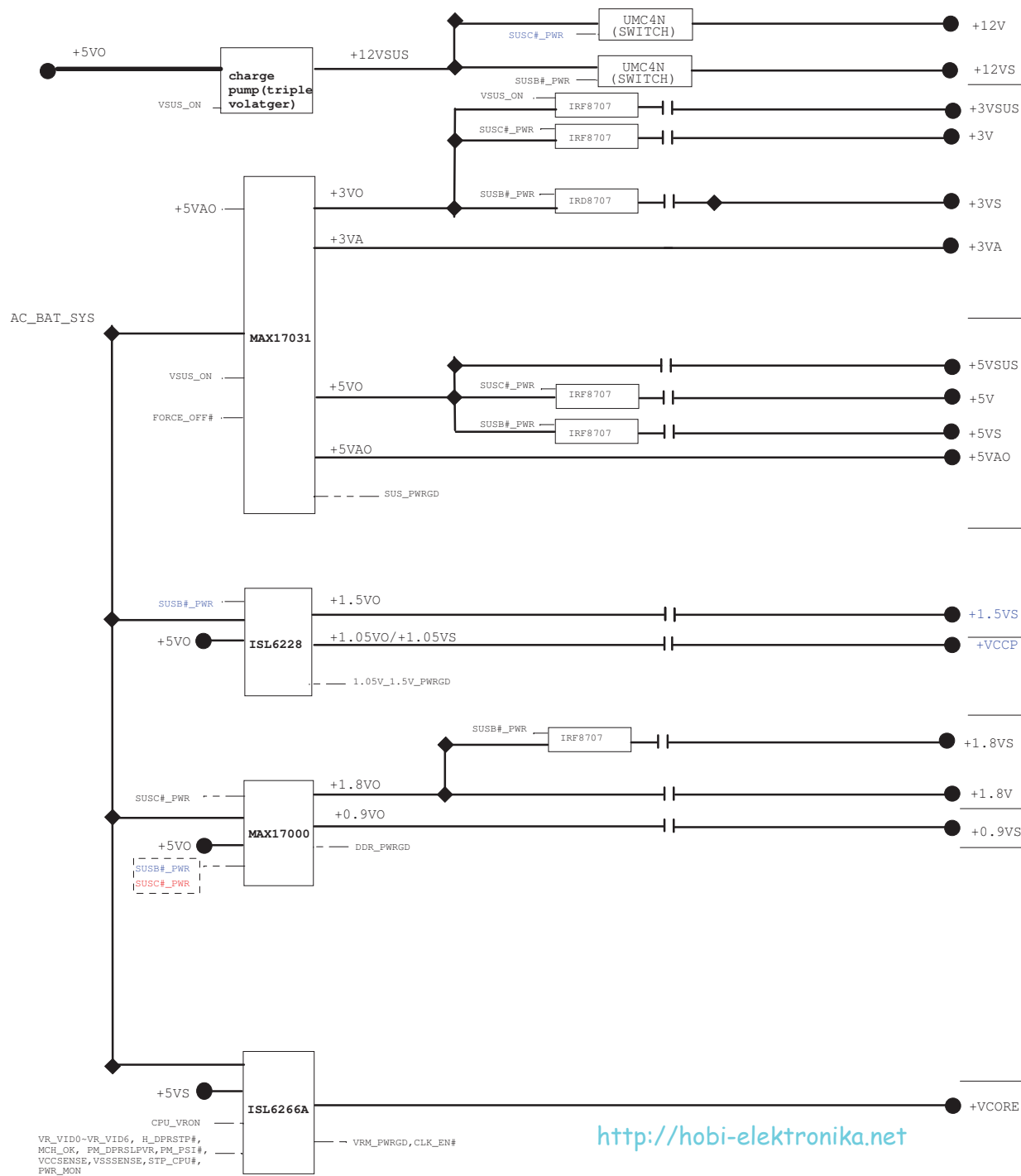
+3VS ○ → +3VS 80,91,92  
 +5VS ○ → +5VS 80,91  
 +12VS ○ → +12VS 91

+1.5VS ○ → +1.5VS 82  
 +0.9VS ○ → +0.9VS 82  
 +1.8VS ○ → +1.8VS 82

+VCCP ○ → +VCCP 82  
 +VCORE ○ → +VCORE 80

## FOR POWER TEST





Design rating	
(10mA)	(20mA)
(10mA)	
(0.74A)	
(1.29A)	
(8.62A)	(10.783A)
(0.133A)	
(0.01A)	
(3.61A)	(7.495A)
(3.875A)	
(0.01A)	
(3.77A)	(3.77A)
(12.816A)	(12.816A)
(11.96A)	(11.96A)
(2A)	(2A)
(47A)	(47A)

<http://hobi-elektronika.net>



R1.0

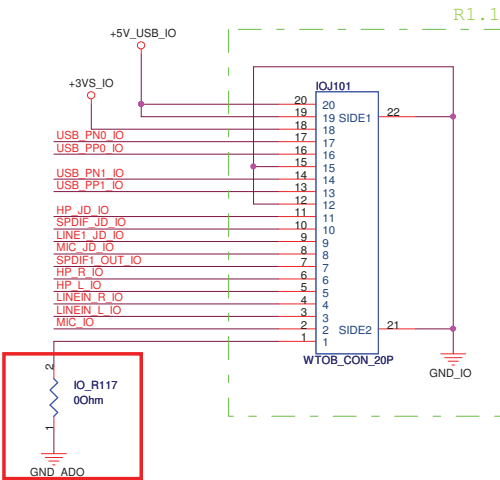
Item	Before	After	Reason	Owner	Date
	R8036:10.5k	R8036 change to 8.87k	To change VCORE load line to meet Intel spec.	Eve Kuo	2008/02/25
	R8015:0805	R8015 from 0805 --> 0603	0805 is common component to use.	Eve Kuo	2008/02/25
	Q8612, R8628, R8629	De-pop Q8612, R8628, R8629	G50V support 3S battery	Eve Kuo	2008/02/25

R1.1

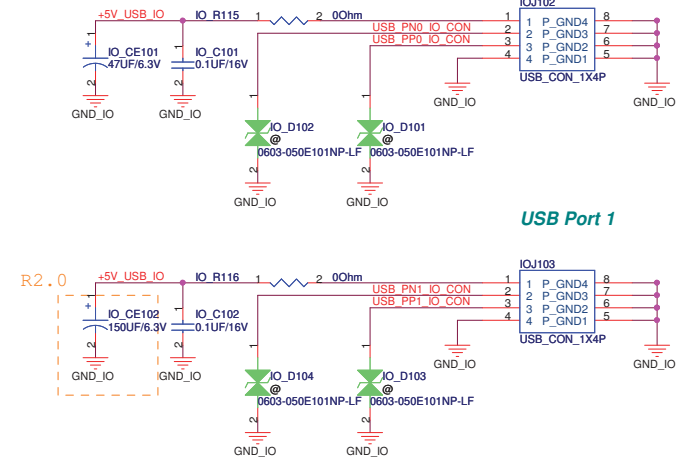
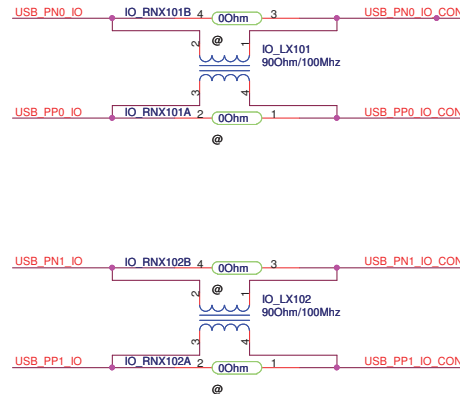
Item	Before	After	Reason	Owner	Date
	JP8601,JP8606	Delete JP8601,JP8606	Due to the factory's requirement, the bead and jump won't be co-lay.		

R2.0

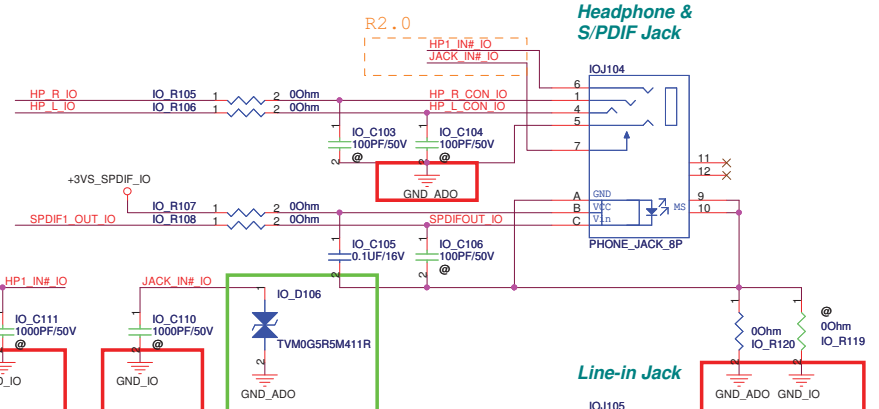
Item	Before	After	Reason	Owner	Date



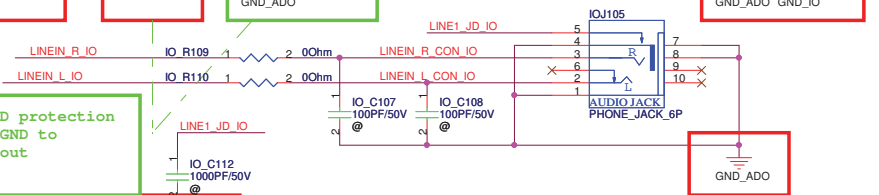
G50VX R1.1: Follow M52VF



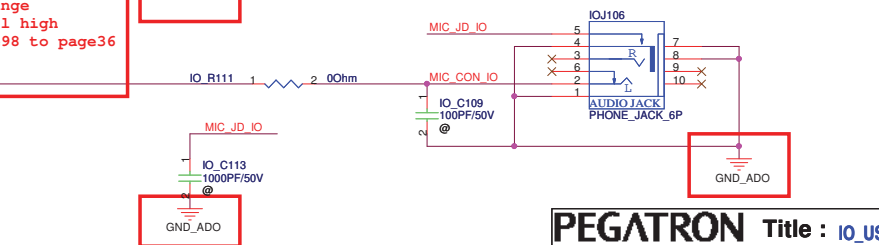
### Headphone & S/PDIF Jack



### Line-in Jack



### MIC In Jack



PEGATRON		Title : IO_USB & Audio Jack	
Pegatron BU2 HW Team 3		Engineer: Kevin1_Guo	
Size	Project Name	G60VX	
Custom		Rev R 1.2	
Date: Wednesday, March 11, 2009	Sheet	98	of 100

# R1.0

## R1.1

### G50VX

2008/02/18	1. Change the port of SATA ODD and SATA HDD to meet design IP. (Page 51) 2. Change SMBus of the Cap-sense Touch key from SMB0 to SMB1. (Page 56) 3. Correct the signals of ESATA. (Page 66) 4. Set R3318 as mount. (Page 33) 5. Correct the signals of PCIE of WLAN. (Page 53) 6. Correct the signals of PCIE of TV Tuner and add the reset signal for PCIE TV Tuner. Set the 1.5V power rail as mount. (Page 64)  7. Unmount pull up resistors of 1394_SCL and 1394_SDA. (Page 40) 8. Add common choke on CMOS for EMI requirement. (Page 45) 9. Correct the signals of Newcard Debug Card. (Page 44) 10. Change the R1407 to 1206 size. (Page 14)
2008/02/20	11. Change EC to 8512. (Page 30) 12. Pull BAT2_IN_OC# up to fix CHARGER_LED bug. (Page 30)
2008/02/21	13. Delete the LCD_BL_DA signal which is designed for Light Sensor. (Page 45) 14. Change the R4504 to 100K to fix LCD will display white screen when system boots. (Page 45)  15. Add uP schematic to control the Game LED for FM request. (Page 69 & 24)
2008/03/05	16. Add discharge circuit for 2.5VS (Page 57) 17. Change BT and WLAN ON/OFF control method (Page 53 and 61) 18. Add ESD Protected Diode on SATA ODD and E-SATA(Page 51 and 66)
2008/03/11	19. Change PEG CLK Source on Clock Gen(Page 29)
2008/03/14	20. Change TouchPad Connector. (Page 31)
2008/03/18	21. Add 2 diodes to follow EC suggestion. (Page 22) 22. Change the IO Connector. (Page 65, 98) 23. Change Power Circuit. (Page 80-94) 24. Exchange CLK_ICHPCI and CLK_KBCPCI to follow Design IP setting. (Page 30) 25. Swap USB Ports to follow Design IP. (Page 45, 52, 64, 68, )
2008/03/19	26. Add 00HM resistor between thermal sensor and CPU to follow Intel Design Guide. (Page 50 ) 27. Add a N-MOS between U4401 and PCI_WAKE# to prevent system can't enter S4 which is waked by U4401. (Page 44 )
2008/03/24	28. Add +3VSUS to NewCard Power Switch. (Page 43) 29. Change the pull-up power source of SMB1 to +3VS. (Page 30)
2008/03/26	30. Change HDD Connector. (Page 51) 31. Add EMI Solution on LVDS connector. (Page 45) 32. Change the Ground of DC Jack for EMI. (Page 60) 33. Add EMI Solution on USB connector. (Page 52) 34. Add EMI Solution on HDMI connector. (Page 48) 35. Add EMI Solution on IO connector. (Page 65) 36. Add EMI Solution on HDD connector. (Page 51) 37. Add EMI Solution on T/P connector. (Page 31)
2008/05/02	38. Correct the Headphone Jack Detect schematic. (Page 98) 39. Change capacitor to MLCC. (Page 33)
2008/05/04	40. Add over-clock strapping. (Page 29)
2008/05/06	41. Reserve Finger Printer Schematic. (Page 63) 42. Add Amplifer strapping. (Page 37) 43. Remove the Capacitor of headphone. (Page 37)

2008/11/17	3. Add comment for supporting Quad Core CPU. (Page 3) 4. Reserve R0411 for support Quad Core, Add BOM option for DC/QC. (Page 4) 5. Add comment for DC/QC. (Page 5) 10. Add comment for DC/QC. (Page 10) 20. Add comment for delete Modem function. (Page 20) 21. Add comment for BOM option. (Page 21) 29. Add comment for CLK Gen BOM option. (Page 29) 30. Change: add Keyboard_LED conntrol signal. (Page 30) 31. Add keyboard LED Power connector, Add comment for delete CIR BOM option (31) 34. Add BOM option for delete RJ11 (34) 35. Add BOM option for delete Modem function (35) 36. Add BOM option for ALC662 and ALC663 co-lay (36) 38. Add BOM option for supporting Array MIC (38) 44. Add BOM option for supporting Debug Connector (44) 45. Add BOM option for supporting Array MIC (45) 50. Add BOM option for Thermal Sensor for QC and DC (50) 63. Add BOM option for deleting FP function. (63) 68. Add BOM option for deleting OLED connector. (68) 69. Co-using of EC.GPA3 pin, for G50V reserved for controlling GAME_LED#. (69)
2008/11/24	31. Change J3103 Pin5, 6 GND name from GND_POWER to GND. (31) 30. Change net GAME_LED_EC# from connecting with EC.GPA3 to EC.GPA6.(30) 68. Delete all the content of page 68: OLED Connector.(68)
2008/11/25	21.Add TP to USBP9N/P.(21) 45.Add F4502 to protect the M/B from demaging by AC_BAT_SYS_INV short to GND; Change C4513 from 0.1UF/16V to 0.1UF/25V.(45) 2008-11-25-21-06
2008/11/26	14.Change C1447 from 0805 to 0603 to satisfy the mechanical height constrain.(14)
2008/12/31	80.Change power solution, related page is 80-84, 86, 90-94
2009/1/2	60.Replace D6002,D6003,D6004 with integrated D6002 for improving the rise time 70.Reserve R7007 for AMD M96 VGA card 33.Add R3323 to reduce the LAN power consumption ?
2009/1/4	36.Change MIC_VREFOUT and 4.7k ohm pull high resistor from page98 to page36, related page is 98, 65, 36  98.isolate the GND_AUDIO and GND_IO 23.Follow Intel DG R2.2, change C2301 from 0.1UF/16V X7R-->1UF/10V X5R 38.change the DSP VDD power to +1.5VS for better immunity of noise and less power 31.change the keyboard connector pin define for chocolate keyboard
2009/1/8	21.Swap USB port 4 and 8, Camera use port 8, newcard use port 4, to decrease the EMI of camera when USB HDD is also used
2009/1/13	80.power team update the schematic  31.Keyboard signal swap for capacitor layout 30.Change EC pin GPH3/ID3 from BAT_LEARN to T3011, delete BAT_LEARN signal 80,81,84. Add net CLK_EN#; Change U8101 symbol; Add R8404 31.Keyboard connector signal change back

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PEGATRON		Title : System History 1	
Pegatron BU2 HW Team 3		Engineer: Kevin1_Guo	
Size Custom	Project Name G60VX		Rev R 1.2
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2009/03/05	Page 23: R2319, R2320 change to 100 ohm (Follow Intel DG R2.2) Page 32: Reserve Force_off# connect to EC_RST# page 41/42: Reserve 10pf capacitor for SD card CLK for EMI Page 43: Add MOS to prevent the leakage current from +3VSUS (U4301 pin 17) to BUF_PLT_RST# page 45: Reserve 33pf capacitor for PWR_LED#, GAME_LED# for EMI Page 45: Change R4501, mount C4503 to tune the falling time of +3VS_LCD Page 46: Follow M52V to change the schematic of RGB to tune the rise/fall time Page 46: Add schematic to protect the HSYNC/VSYNC from pulling low by CRT connector for M52VP Page 48: Reserve schematic for G50VX HDMI HPD signal level shift Page 48: Reserve pull high resistor and decoupling capacitor for TMDS signals Page 53: change WLAN pin 39,41 from NC to 3.3V power for full support Intel WiFi Link Page 69: Change GAME_LED# control from PIC MCU to EC Page 70: Reserve bead for MXM card for EMI Page 81: Reserve D8107 to prevent leakage from +3V, +3VS to +3VSUS and ENBL when VSUS_ON accidentally pulled low  Page 98: Reserve VPORT (varistor) on signal HP1_IN#_IO and JACK_IN#_IO for ESD protection
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